Signal Processing Electronics

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Plan of the course

- Lecture – 1
  - Basic concepts, from signals to DAQ systems
- Lecture – 2
  - Signal transmission, preamplifiers, shaping amplifiers, discriminators, coincidence circuits and instrumentation standards
- Lecture – 3
  - Analog-to-Digital, Time-to-Digital Converters and modern DAQ system elements
- Examples from CMS, ALICE and INO experiments

Part-III

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Acknowledgements & References: G.Hall, W.R.Leo, JÖrgen Christiansen, GRAPES collaboration , Ortec, P.Horowitz & W.Hill, C.F.G.Delaney

Analogue to Digital Conversion

- Turns electrical input (voltage/current) into numeric value
- Parameters and requirements
  - Resolution
    - the granularity of the digital values
  - Integral Non-Linearity
    - proportionality of output to input
  - Differential Non-Linearity
    - uniformity of digitisation increments
  - Conversion time
    - how much time to convert signal to digital value
  - Count-rate performance
    - how quickly a new conversion can begin after a previous event
  - Stability
    - how much values change with time

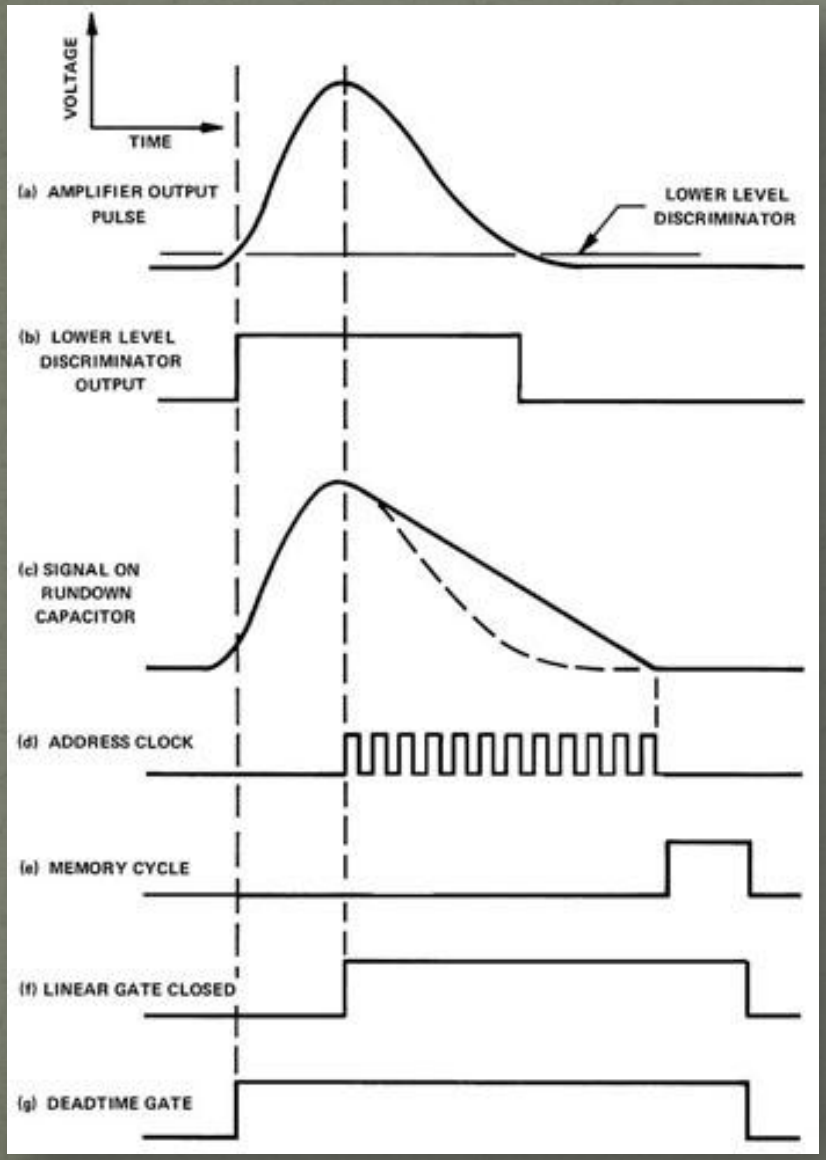
Analog-to-Digital Converters (ADCs)

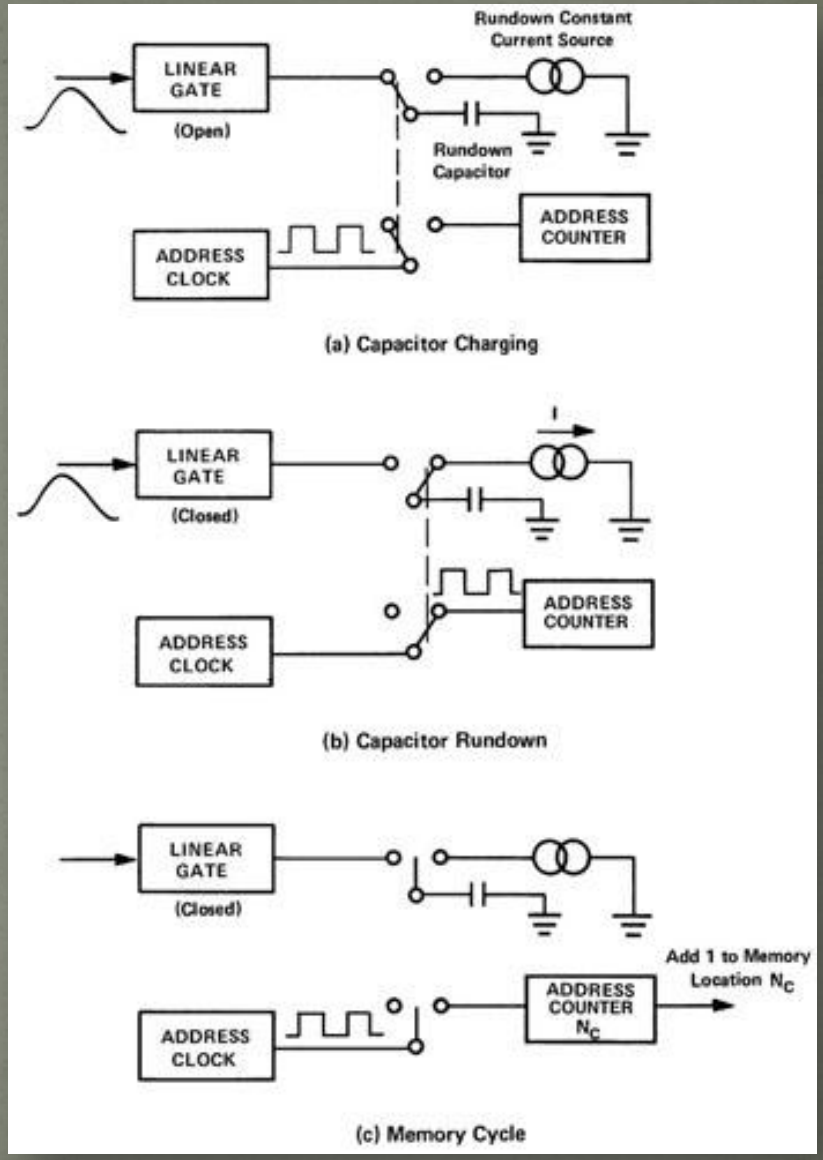
- Peak-sensing
  - Maximum of the voltage signal is digitised
  - Ex: Signal of the PMT in voltage mode (slow signals, already integrated)
- Charge sensitive
  - Total integrated current digitised
  - Ex: Signal of the PMT in the current mode (fast signals)
- Time of integration or the time period over which the ADC seeks a maximum is determined by the width of the gate signal

Types of ADCs

- Ramp or Wilkinson
- Successive approximation
- Flash or parallel
- Sigma-delta ADC
- Hybrid (Wilkinson + successive approximation)
- Tracking ADC
- Parallel ripple ADC
- Variable threshold flash ADC
- …

Ramp or Wilkinson ADC





Successive approximation ADC

- analogous to binary search

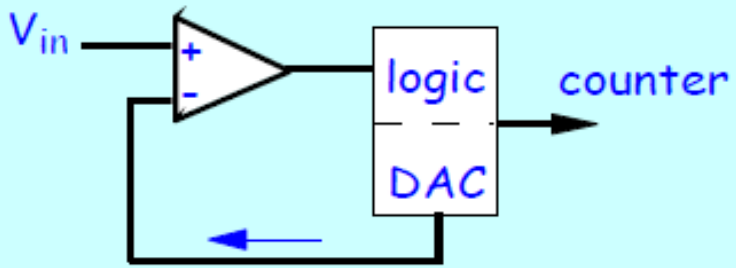
  generate $V_{ref} = \Delta V \times (2^{N-1}, 2^{N-2}, \ldots 2^0)$ in N steps

  set bit = 1

  if $V_{in} > V_{ref}$

  leave

  else bit = 0



- Pros

  speed ~ μsec

  high resolution

- Cons

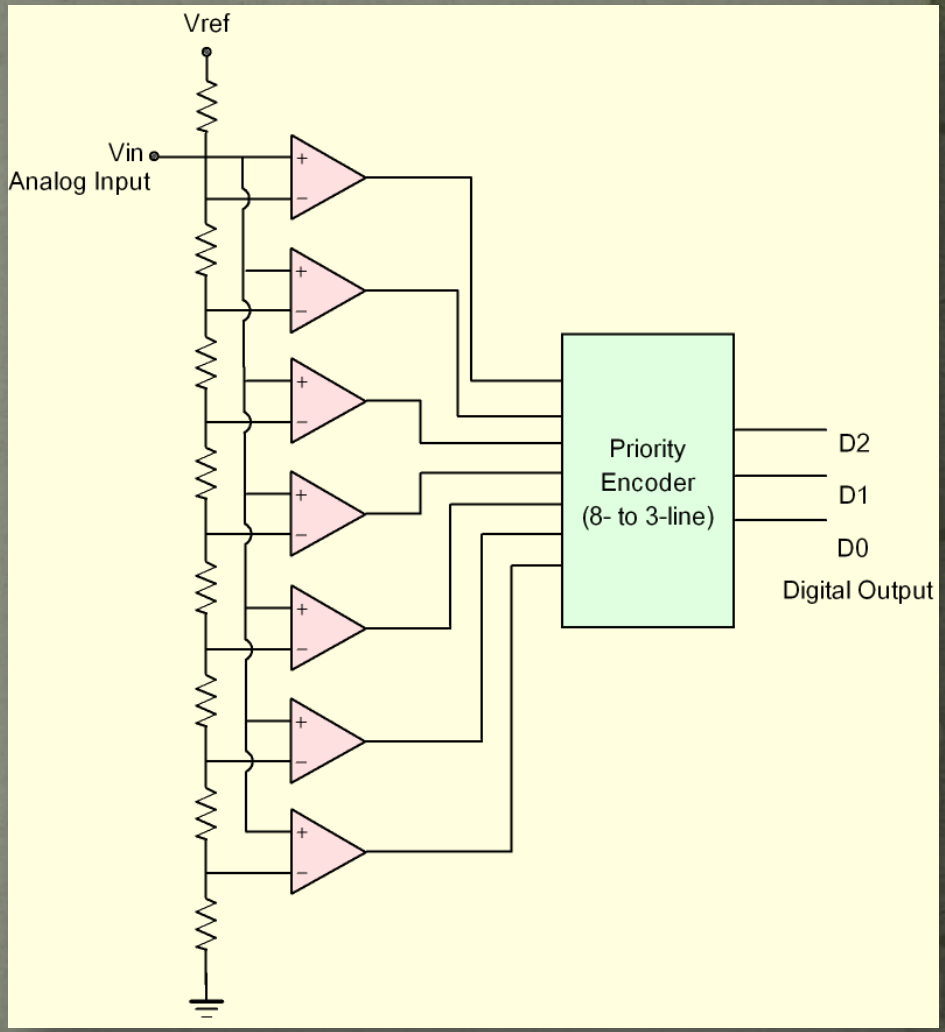
  DNL 10-20%

  very precise resistors required with DAC for V_{ref}

DAC = digital to analogue converter
ie number -> voltage

Flash or parallel ADC

- Flash ADC is the fastest ADC type available. The digital equivalent of the analog signal will be available right away at it output – hence the name “flash”.
- The number of required comparers is 2^{n-1}, where n is the number of output bits.
- Since Flash ADC comparisons are set by a set of resistors, one could set different values for the resistors in order to obtain a non-linear output, i.e. one value would represent a different voltage step from the other values.



Sigma-delta ADC

- Digitise the signal with 1-bit resolution at a high sampling rate (MHz).

  useful for high resolution conversion of low-frequency signals, to 20bits

  low-distortion conversion of audio signals

  good linearity and high accuracy.

- Operation - At t = 0, assume V_{ref} = 0

  V_{out} high

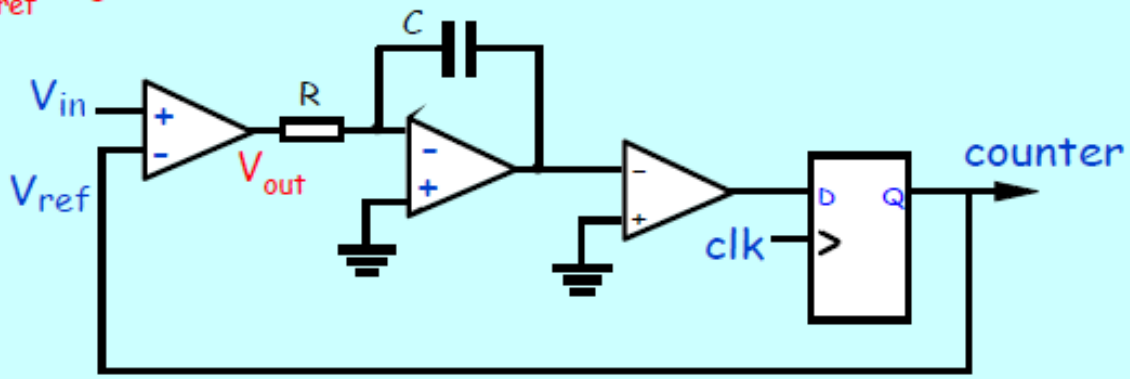
  integrator charges -ve

  at rate ~ V_{in}

  comparator flips

  counter goes low

  clock increments... etc,...



V_{in} = 0 => output = 000000...

V_{in} = (1/2)V_{in}(max) => output = 101010...

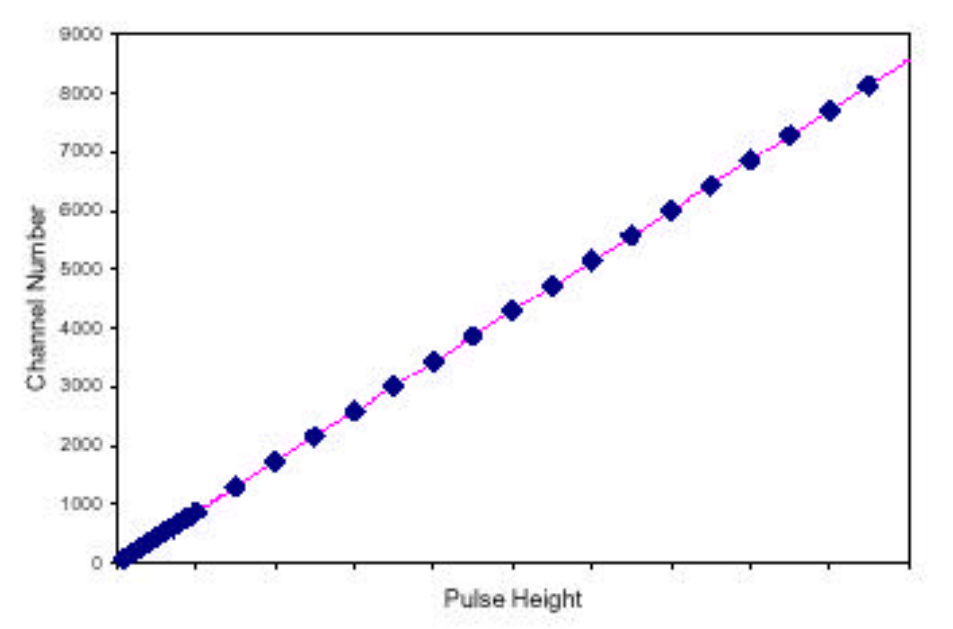
V_{in} = V_{in}(max) => output = 111111...

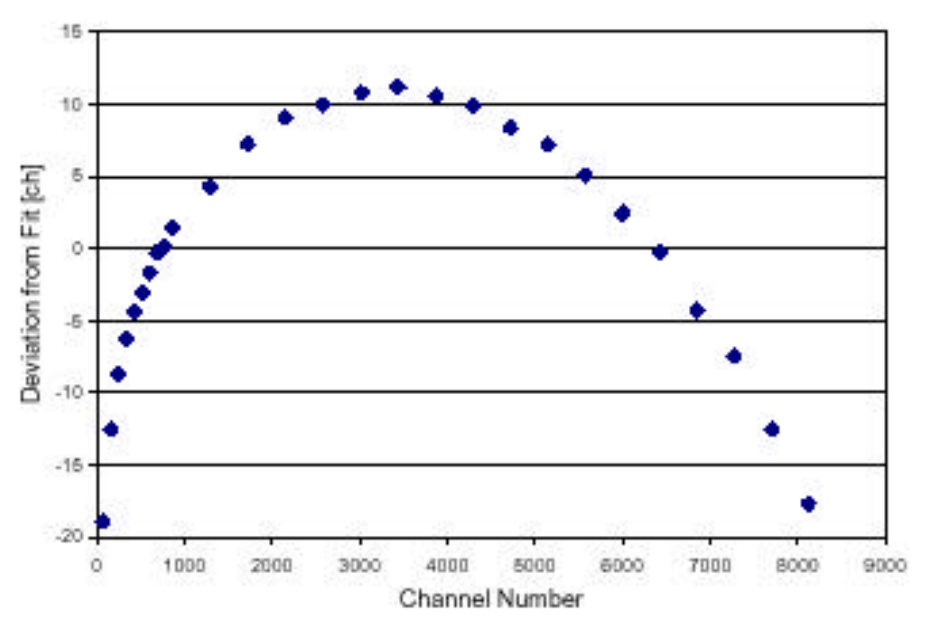
the higher the input voltage, the more 1's at the serial digital output.

Integral non-linearity

- Output value D should be linearly proportional to V
- Check with plot

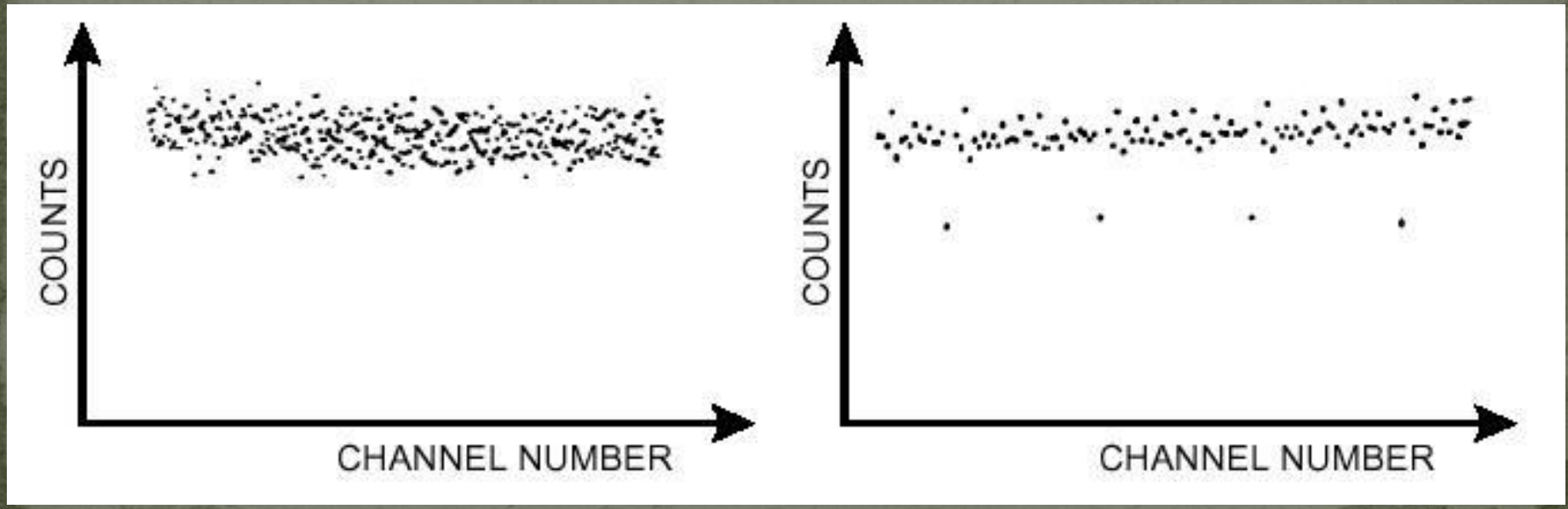
- For more precise evaluation of INL fit to line and plot deviations
- Plot D_i-D_{fit} vs nchan





Differential non-linearity

- Measures non-uniformity in channel profiles over range
  DNL = $DV_i/\langle DV \rangle - 1$
  DV_i = width of channel i
  $\langle DV \rangle$ = average width
- RMS or worst case values may be quoted
  DNL ~ 1% typical but 10^{-3} can be achieved
  can show up systematic effects, as well as random



Resolution

- To convert an analogue value, eg voltage, to digital two parameters are required

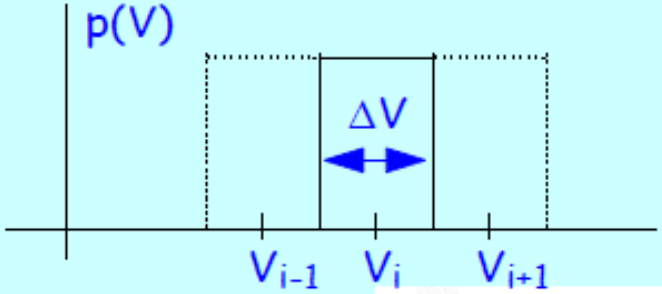
  range and number of bits

  quantum = $\Delta V = (V_{max}-V_{min})*2^{-N}$ referred to as 1LSB (least significant bit)

- eg 10 bits = $2^{10} = 1024$, $V_{max}-V_{min} = 1V$ => $\Delta V = 1V/1024 \approx 1mV$

- Ideal ADC behaviour

  probability vs amplitude

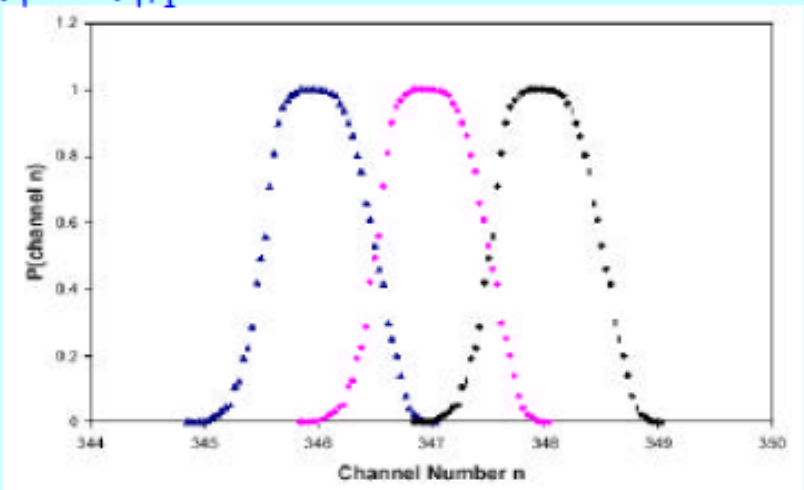


- Real ADC behaviour

  noise in digitisation process

  smears resolution

$\sigma_{noise} < \Delta V/4$



Other variables

- Conversion time
  - finite time is required for conversion and storage of values
  - may depend on signal amplitude
  - gives rise to dead time in system
  - i.e. system cannot handle another event during dead time
  - may need accounting for, or risk bias in results
- Rate effects
  - results may depend on rate of arrival of signals
  - typically lead to spectral broadening
- Stability
  - temperature effects are a typical cause of variations
- A partial solution to most of these problems is regular calibration, preferably under real operating conditions, as well as control of variables

Non-linear ADC

- A integrating system for measuring x-ray photons for crystallography, measuring spots. The most intense spots contain up to ~10^9 photons, the weakest just a few. Measure N in spot

  aim: achieve 1% resolution

  using a 10-bit ADC (cost)

  assume 1V range

  1V = largest signal, defines G_1

  $N < 10^4$ $\sigma(N)/N > 1\%$

  defines smallest signals

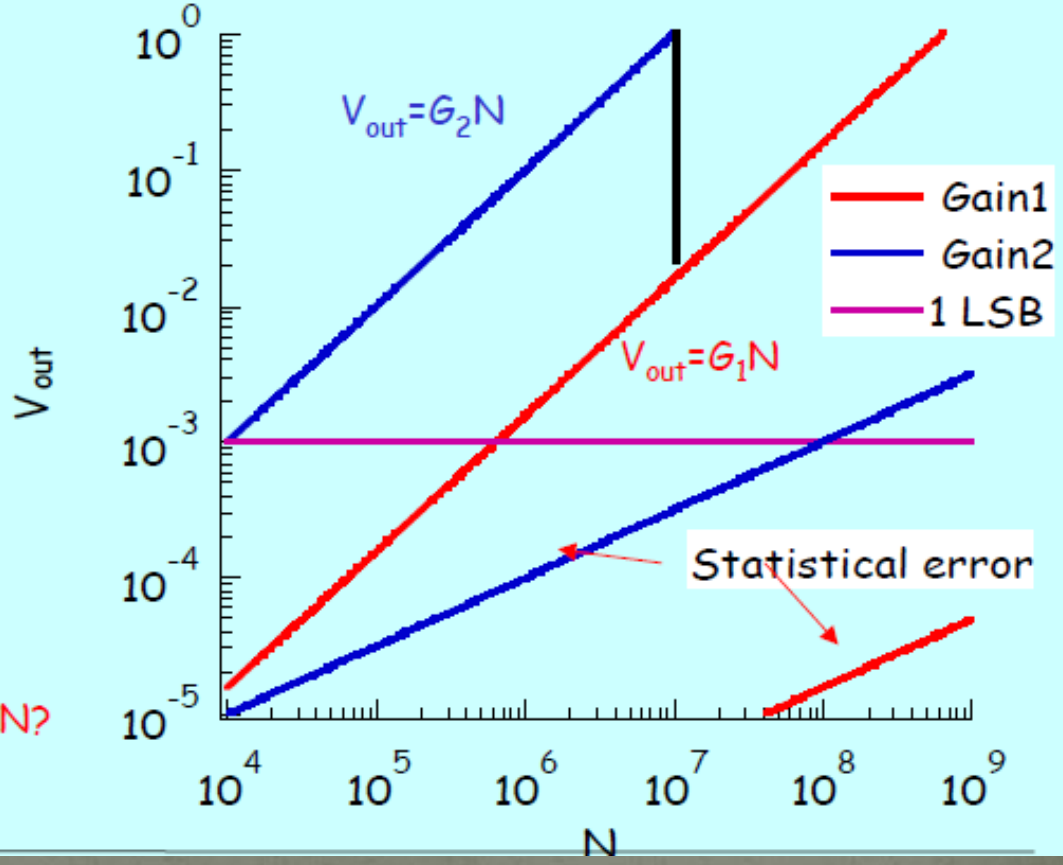
  but ADC LSB > signal

  Increase small signal gain G_2

  Select output in ADC range

- Is 1% resolution achieved for all N?

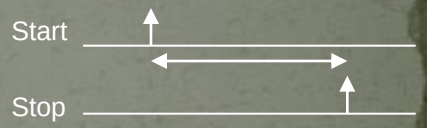
  If not… ?

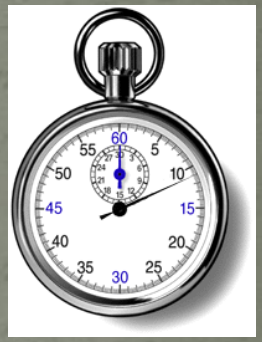


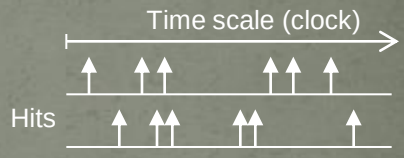
Why TDCs?

TDCs are used to measure time or intervals

- Start – Stop measurement
  - Measurement of time interval between two events:
    Start signal – Stop signal
  - Used to measure relatively short time intervals with high precision
  - Like a stop watch used to measure sport competitions
- Time tagging
  - Measure time of occurrence of events with a given time reference:
    Time reference (Clock)
    Events to be measured (Hits)
  - Used to measure relative occurrence of many events on a defined time scale:
    Such a time scale will have limited range; like 12/24 hour time scale on your watch when having no date and year







Where TDCs?

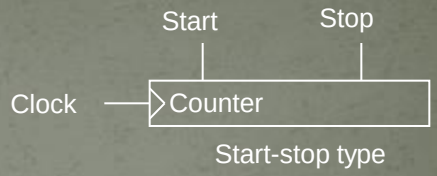
- Special needs for High Energy Physics
  - Many thousands of channels needed
  - Rate of measurements can be very high
  - Very high timing resolution
  - A mechanism to store measurements during a given interval and extract only those related to an interesting event, signaled by a trigger, must be integrated with TDC function
- Other applications
  - Laser/radar ranging to measure distance between cars
  - Time delay reflection to measure location of broken fiber
  - Most other applications only needs one or a few channels

How to compare TDCs?

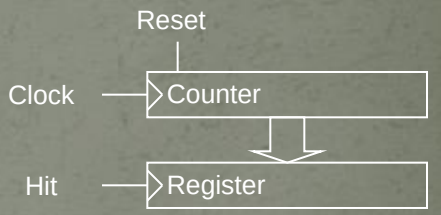
- Merits
  - Resolution
    - Bin size and effective resolution (RMS, INL, DNL)
  - Dynamic range
  - Stability
    - Use of external reference
    - Drift (e.g. temperature)
    - Jitter and Noise
  - Integration issues
    - Digital / analog
    - Noise / power supply sensitivity
    - Sensitivity to matching of active elements
    - Required IC area
    - Common timing block per channel
    - Time critical block must be implemented on chip together with noisy digital logic
- Use in final system
    - Can one actually use effectively very high time resolution in large systems (detectors)
    - Calibration - stability
    - Distribution of timing reference (start signal or reference clock)
    - Other features: data buffering, triggering, readout, test, radiation, etc.

Basic TDC types - I

- Counter type
  - Advantages
    - Simple; but still useful!
    - Digital
    - large dynamic range possible
    - Easy to integrate many channels per chip
  - Disadvantages
    - Limited time resolution (1ns using modern CMOS technology)
    - Meta stability (use of Gray code counter)
- Single Delay chain type
  - Cable delay chain (distributed L-C)
    - Very good resolution (5ps mm)
    - Not easy to integrate on integrated circuits
  - Simple delay chain using active *gates*
    - Good resolution (~100ps using modern tech)
    - Limited dynamic range (long delay chain and register)
    - Only start-stop type
    - Large delay variations between chips and with temperature and supply voltage

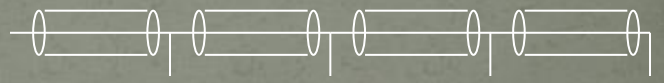


Start-stop type

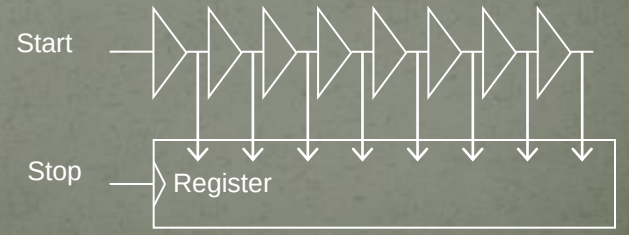


Time tagging type

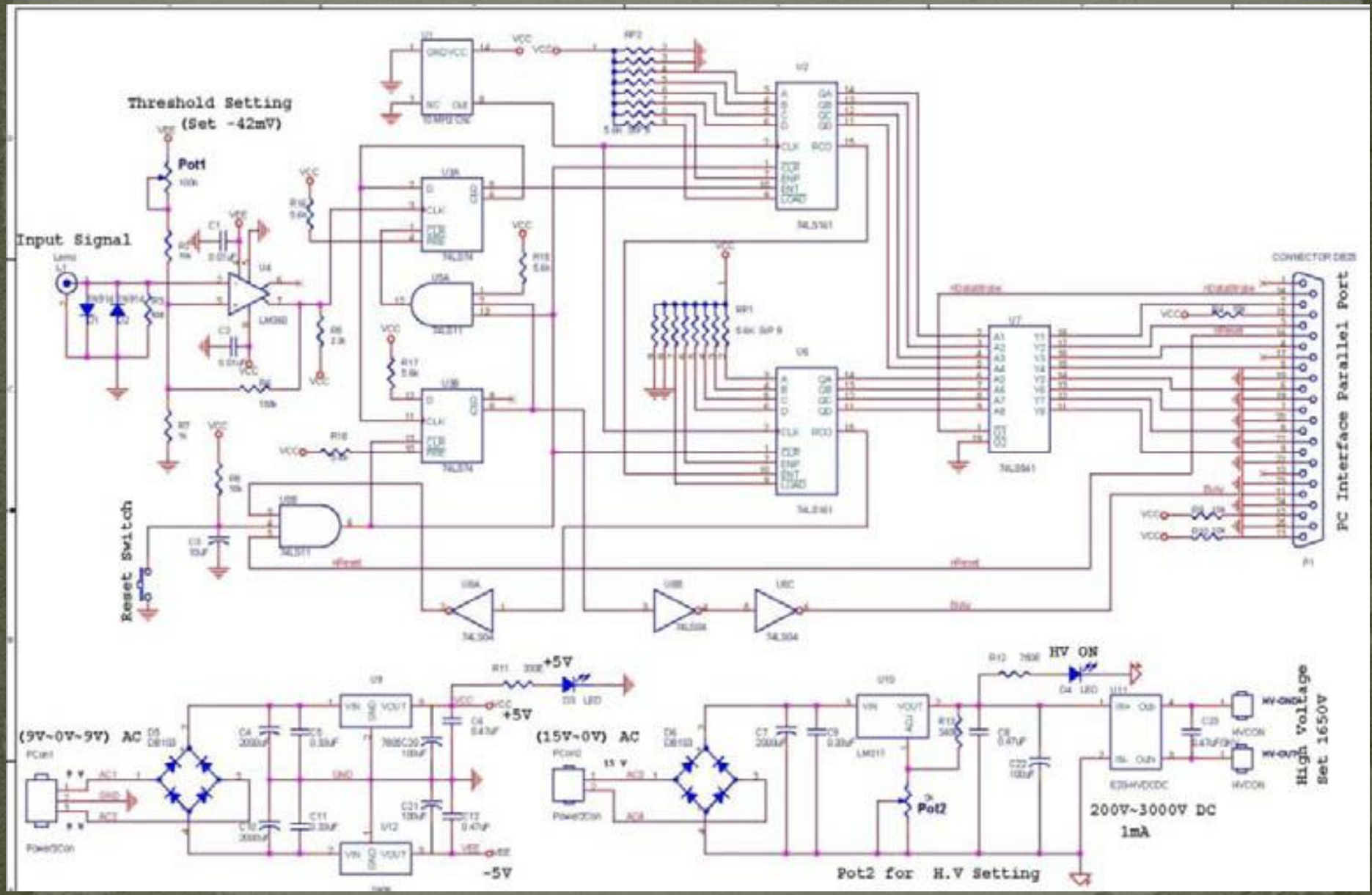
Cable delay chain



Delay chain with non-inverting gates

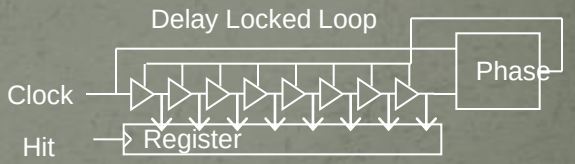


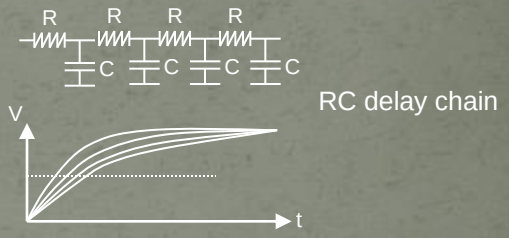
Counter-type TDC



Basic TDC types - II

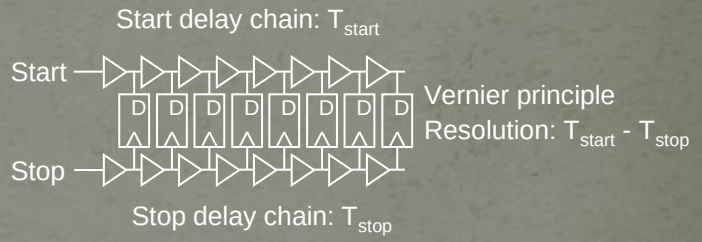
- Single Delay chain type (Contd …)
  - Delay locked loop
    - Self calibrating using external frequency reference (clock)
    - Allows combination with counter
    - Delicate feedback loop design (jitter)
  - R-C delay chain
    - Very good resolution
    - Signal slew rate deteriorates
    - Delay chain with losses; so only short delay chain possible
    - Large sensitivity to process parameters (and temperature)

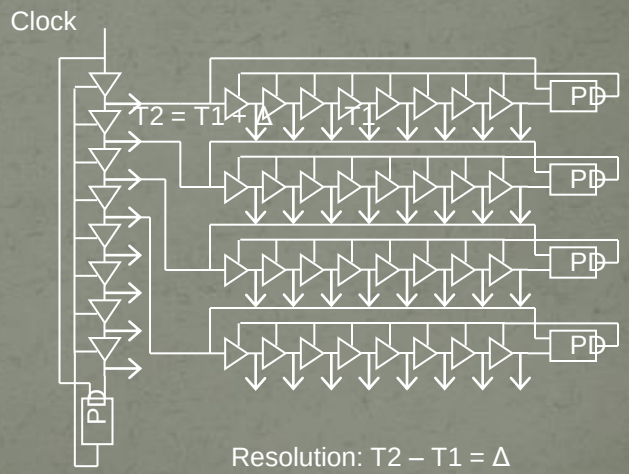




Basic TDC types - III

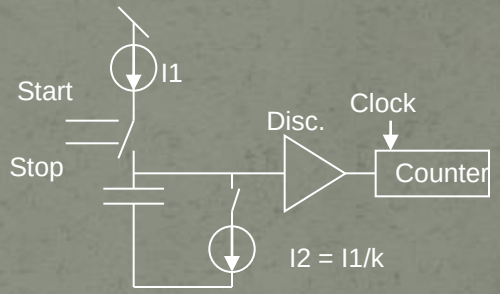
- Multiple delay chain type
  - Vernier delay chain types
    - Resolution determined by delay difference between two chains. Delay difference can be made very small and very high resolution can be obtained.
    - Small dynamic range (long chains)
    - Delay chains can not be directly calibrated using DLL
    - Matching between delay cells becomes critical
  - Coupled delay locked loops
    - Sub-delay cell resolution (¼)
    - All DLLs use common time reference (clock)
    - Common timing generator for multiple channels
    - Jitter analysis not trivial

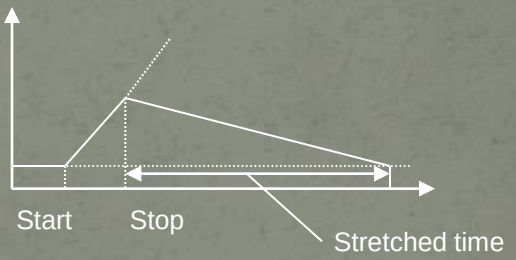




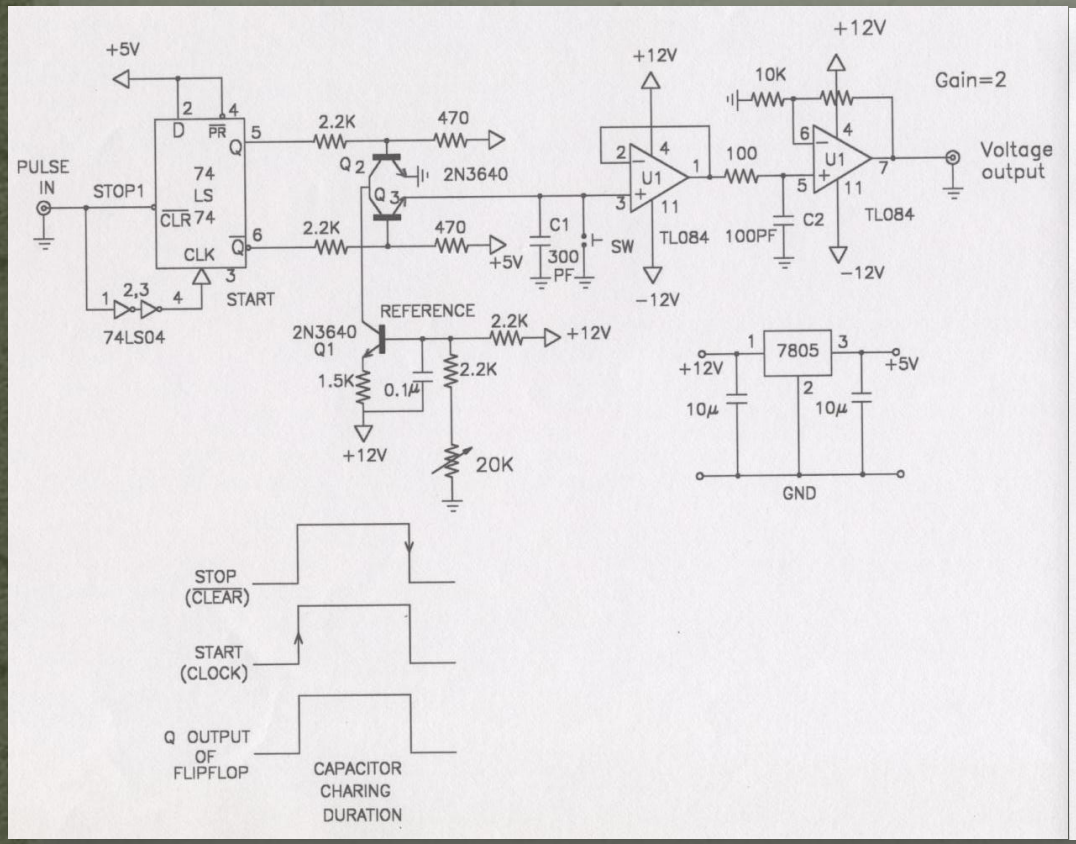
Basic TDC types - IV

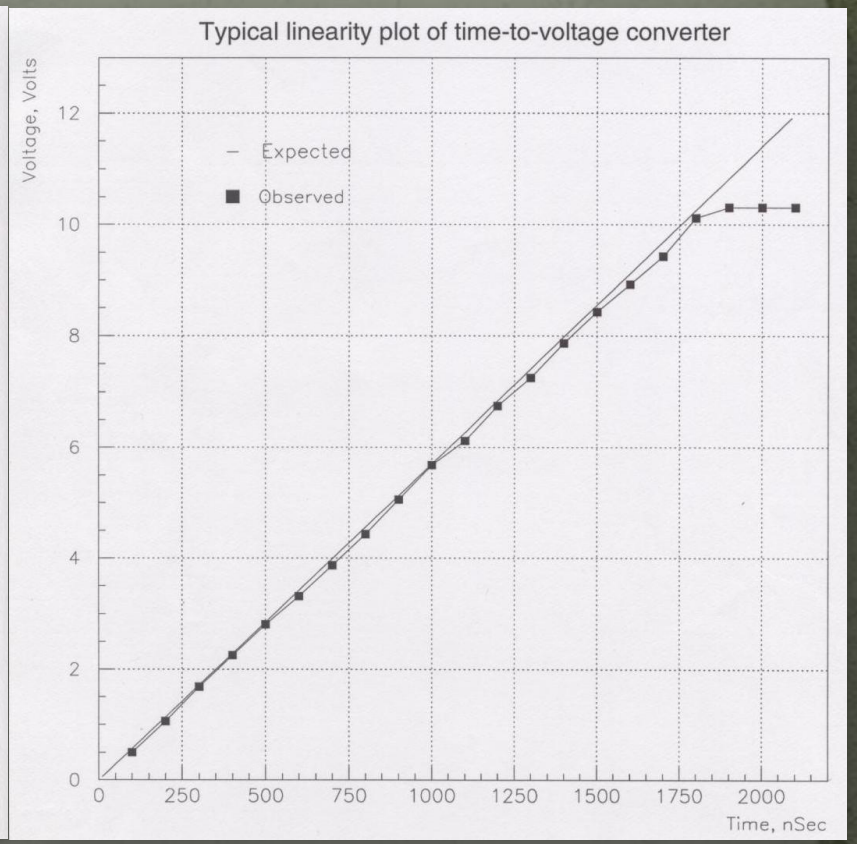
- Charge integration
  - Using ADC (TAC)
    - High resolution
    - Low dynamic range
    - Sensitive analog design
    - Low hit rate
    - Requires ADC
  - Using double slope (time stretcher)
    - No need for ADC (substituted with a counter)
- Multiple *exotic* architectures
  - Heavily coupled phase locked loops
  - Beating between two PLLs
  - Re-circulating delay loops
  - Summing of signals with different slew rates



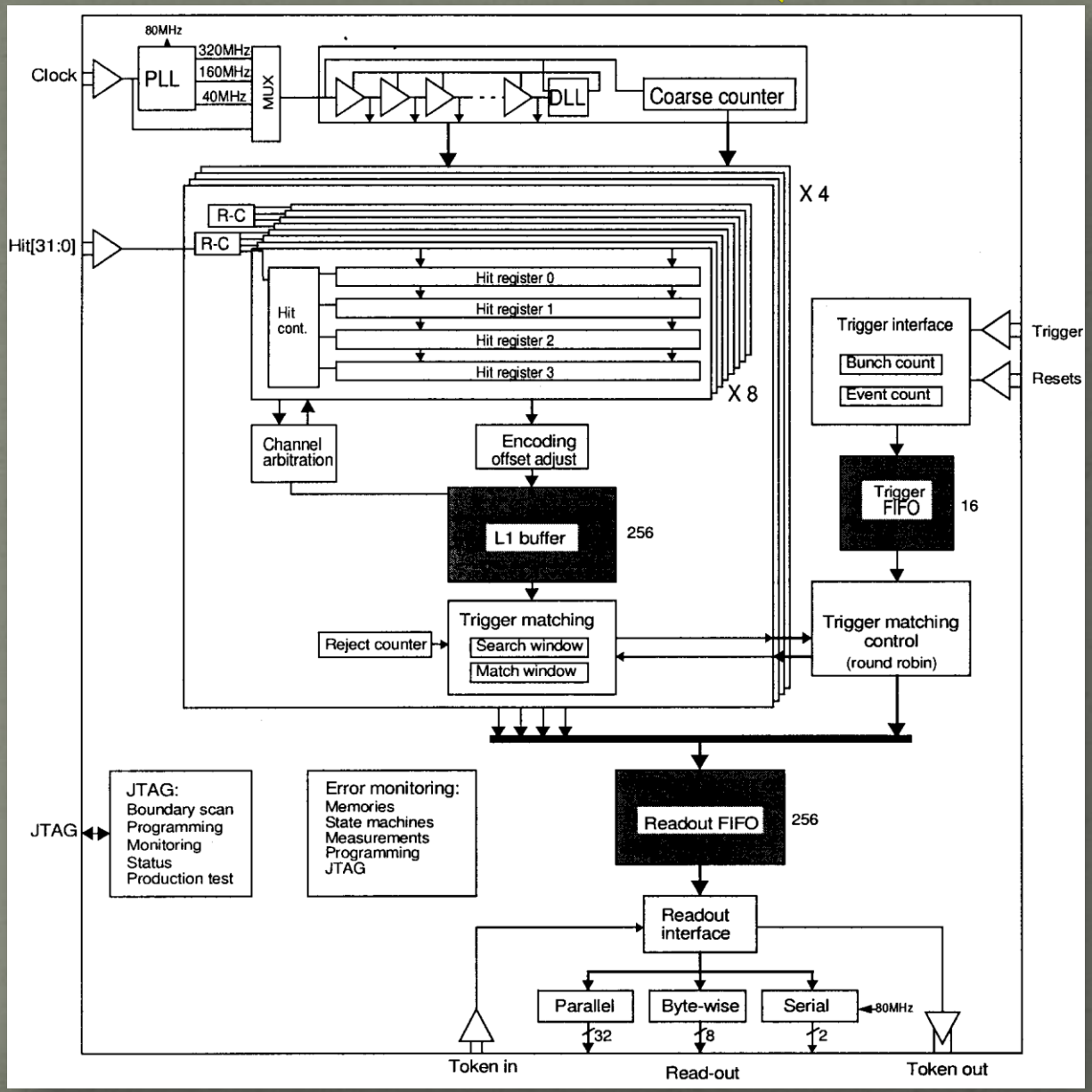


Time-to-Amplitude Converter (TAC)



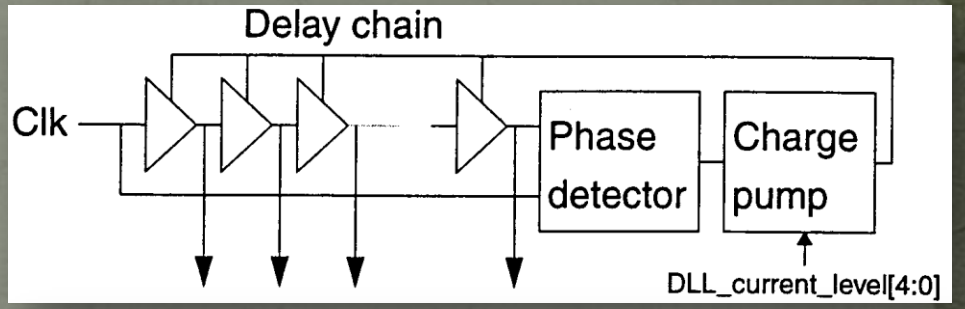


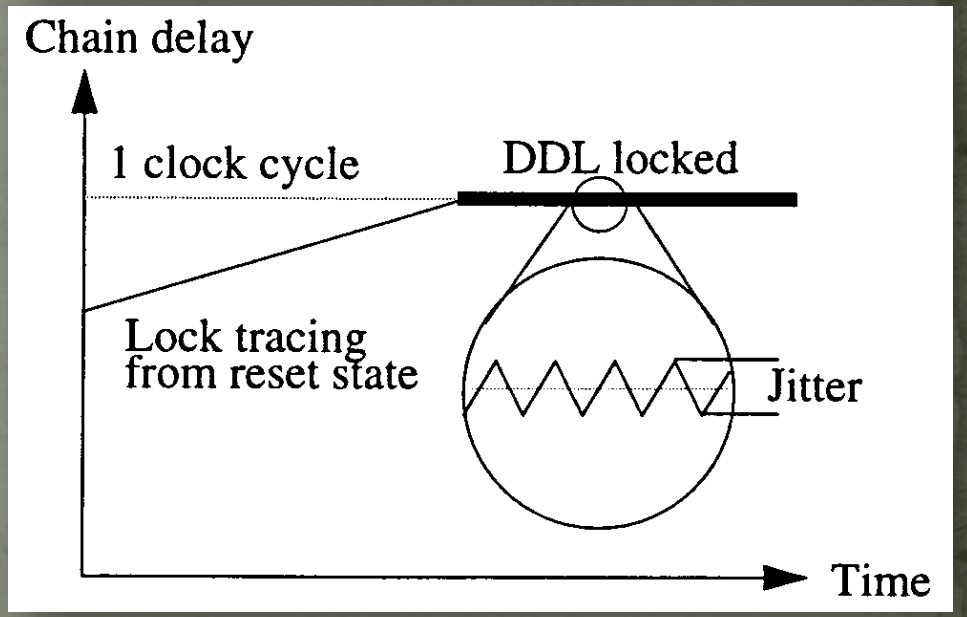
Architecture of HPTDC (ALICE TOF)



Delay Locked Loop (DLL)

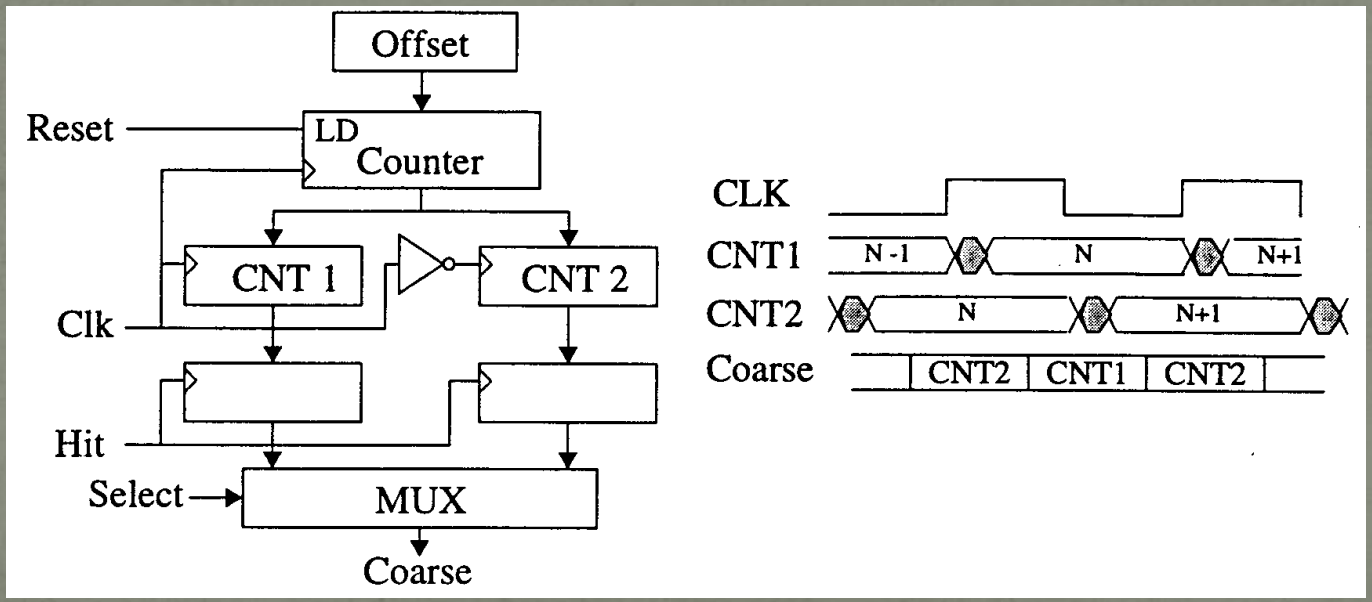
- Three major components:
  - Chain of 32 delay elements; adjustable delay
  - Phase detector between clock and delayed signal
  - Charge pump & level shifter generating control voltage to the delay elements
- Jitter in the delay chain
- Lock monitoring
- Dynamics of the control loop
- Programmable charge pump current level

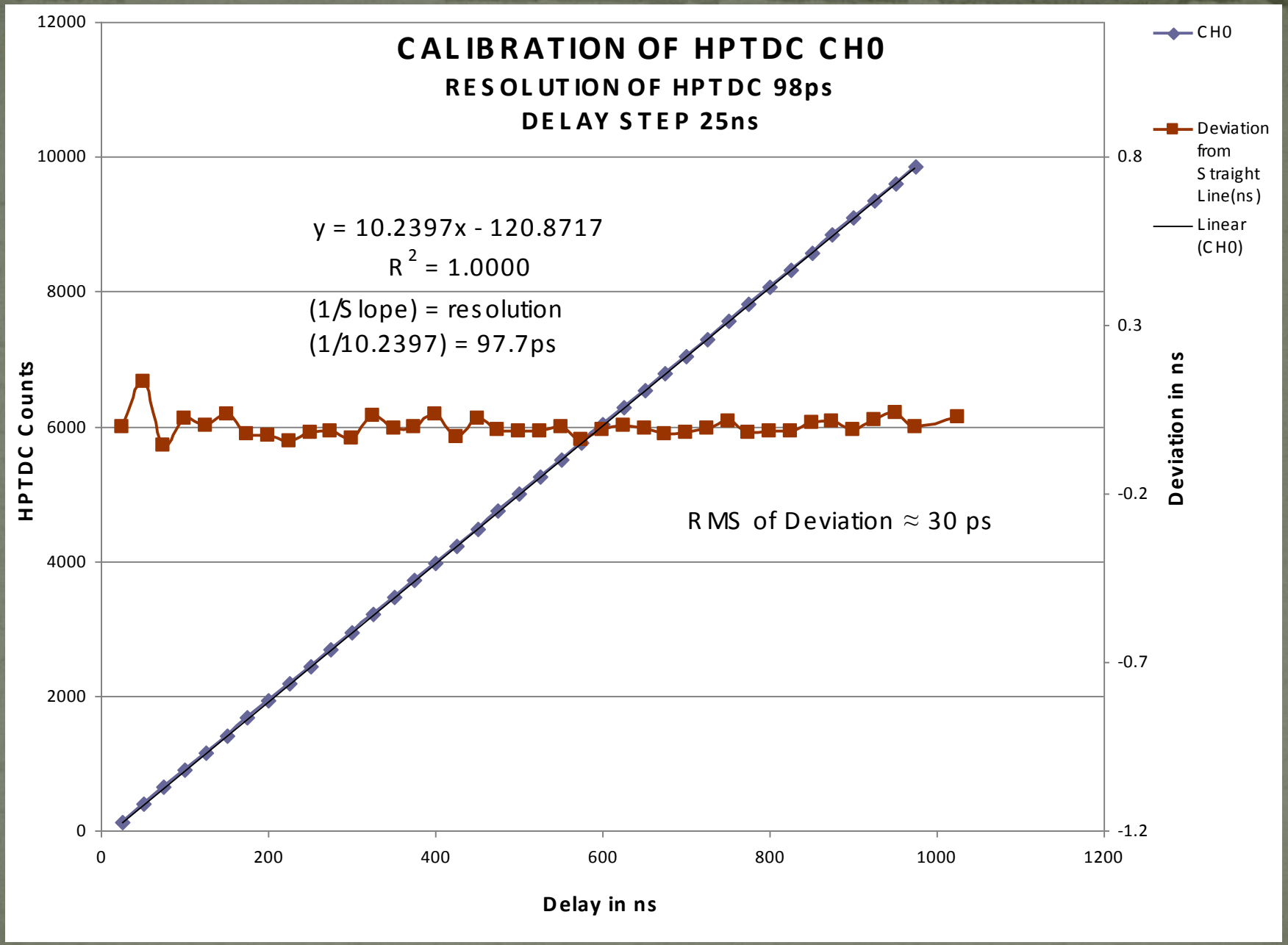




Coarse time count

- Dynamic range of the fine time measurement, extracted from the state of DLL is expanded, by
- Storing the state of a clock synchronous counter
- Hit signal is synchronous to the clocking, so
- Two count values, ½ a clock cycle out of phase stored
- At reset, coarse time counter loaded with time offset

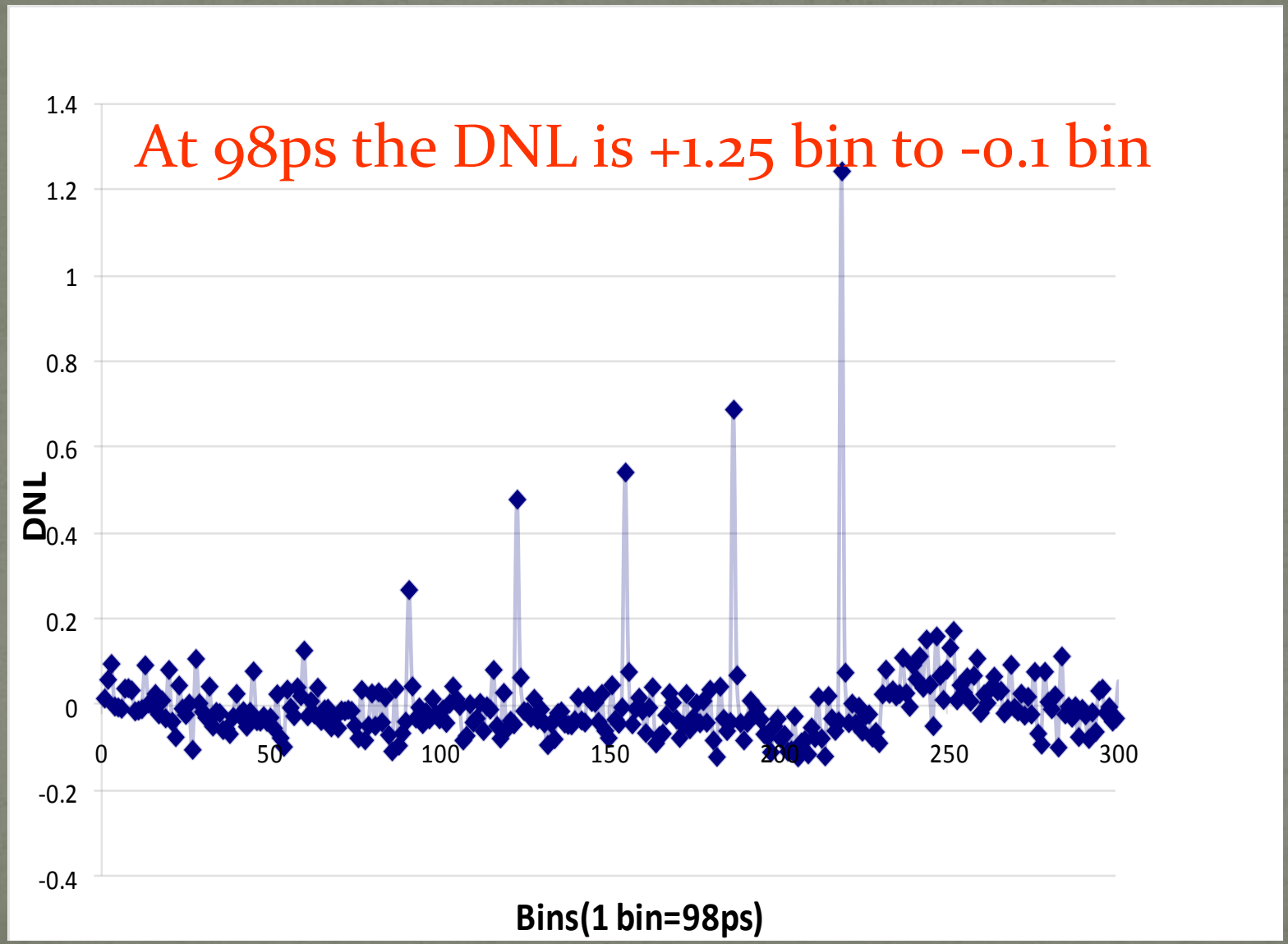



CALIBRATION OF HPTDC CH0
RESOLUTION OF HPTDC 98ps
DELAY STEP 25ns
y = 10.2397x - 120.8717
R 2 = 1.0000
(1/Slope) = resolution
(1/10.2397) = 97.7ps
RMS of Deviation ≈ 30 ps
HPTDC Counts
Delay in ns
Deviation in ns
CH0
Deviation from Straight Line(ns)
Linear (CH0)
12000
10000
8000
6000
4000
2000
0
200
400
600
800
1000
1200
0.8
0.3
-0.2
-0.7
-1.2

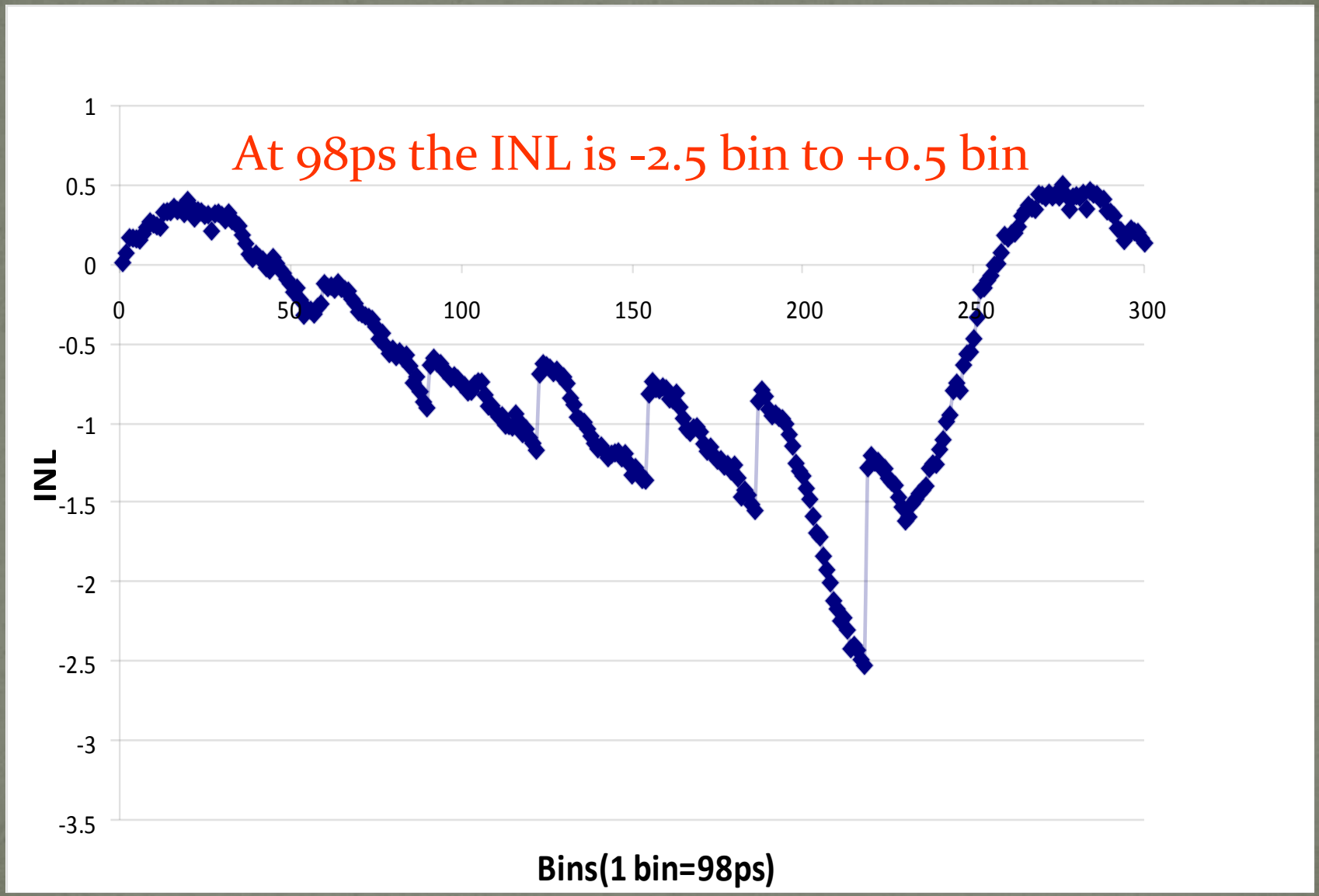
HPTDC's DNL and INL

- Differential Non-Linearity(DNL) is defined as the variation of any code from an ideal 1 LSB step.
- DNL(n) = (Actual(n)/Expected(n)) – 1.
- Integral Non-Linearity (INL) is the deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line. INL is simply the integral of the DNL.
- So if we can get the DNL then we can compute the INL.
- In HPTDC the base clock is 40 MHz i.e. 25ns so the DNL pattern repeats every 25ns.

HPTDC's DNL test result



HPTDC's INL test result



HPTDC's DNL/INL data correction

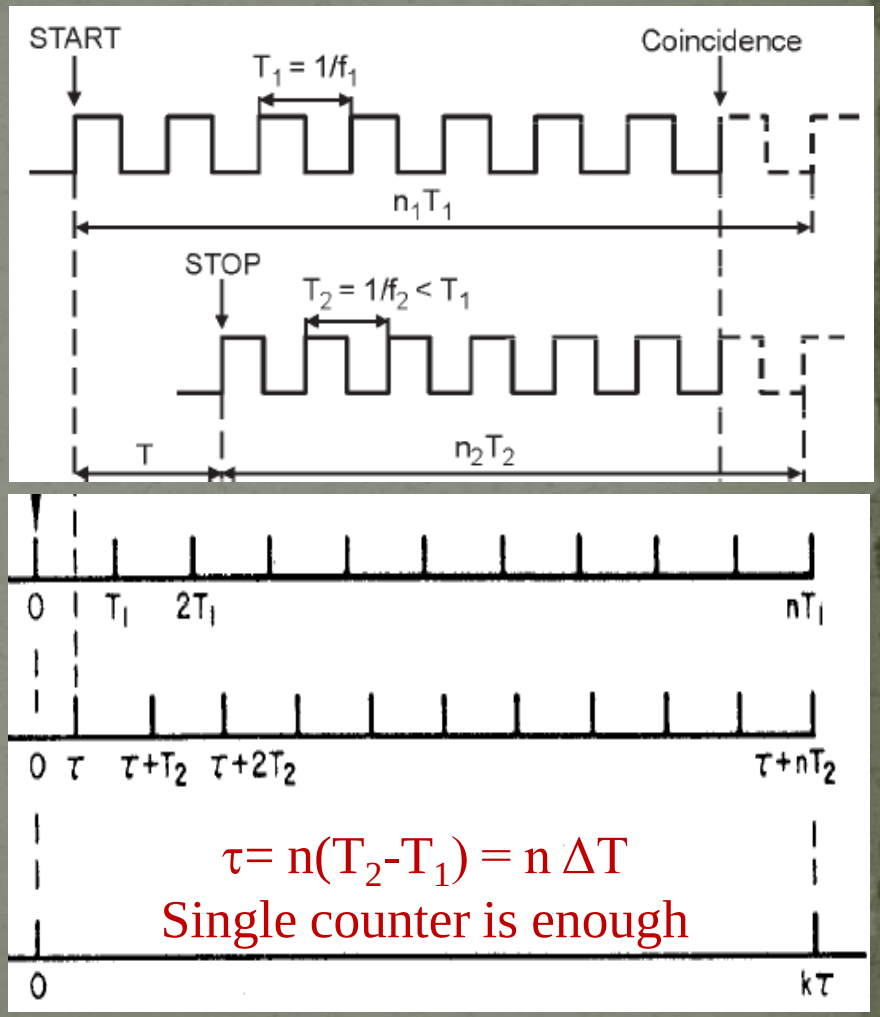
- The fixed pattern in the INL is caused by 40 MHz cross talk from the logic part of the chip to the time measurement part .
- As this crosstalk comes from the 40MHz clock, which is also the time reference of the TDC, the integral non linearity have a stable shape between chips and can therefore be compensated for using the LSB bits of the measurements.

Test Condition	Effective resolution (RMS)
98ps resolution	64ps
98ps resolution after INL correction	34ps
24ps resolution	58ps
24ps resolution after INL correction	17ps

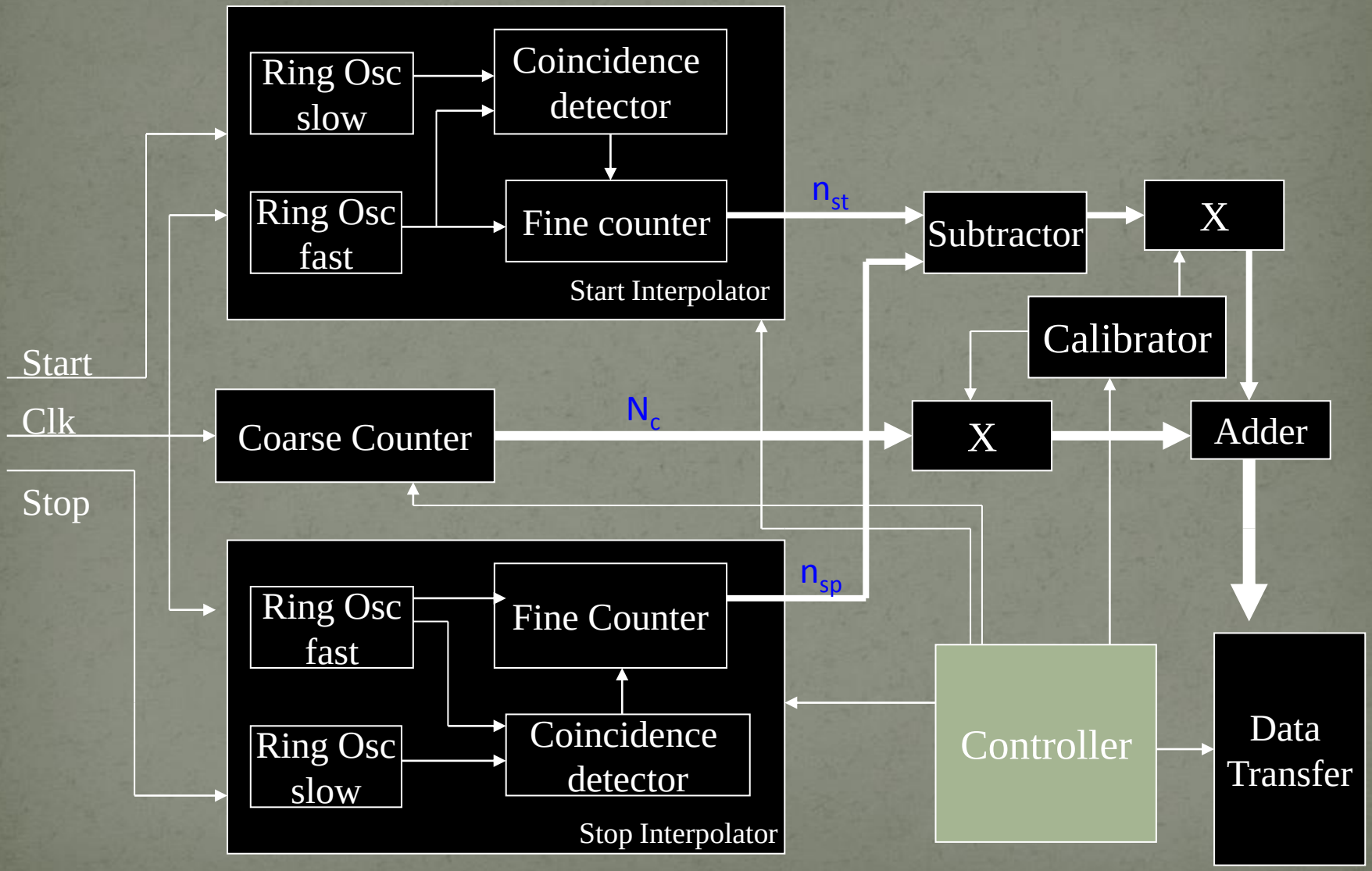
Concept of vernier TDC

- Two clocks of slightly different periods T_1 and T_2 ($T_1 > T_2$) are employed.
- START pulse will start the slow oscillator(T_1) and STOP pulse will start the fast oscillator (T_2).
- Since $T_2 < T_1$, fast oscillator will catch up with the slow one.
- The time interval between the START and STOP can be measured as:

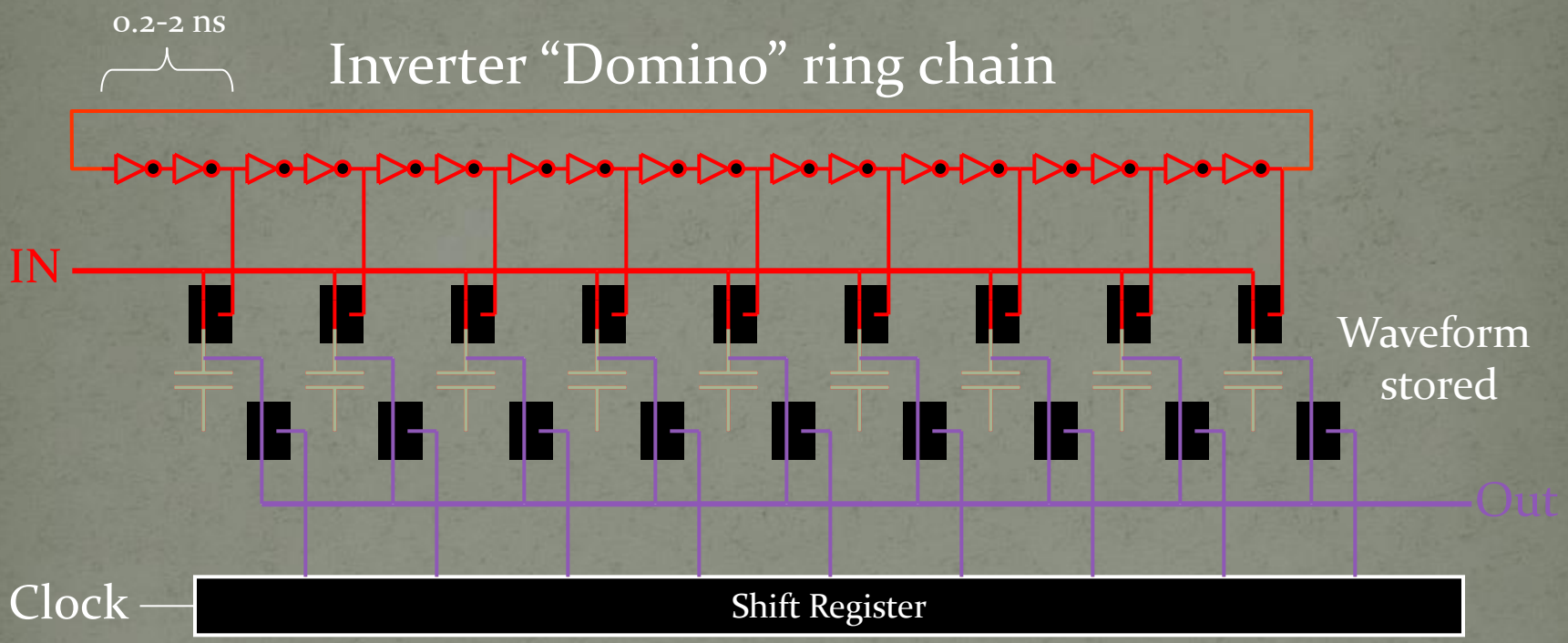
  $T = (N_1 - 1)\,T_1 - (N_2 - 1)\,T_2$
- Two counters for N_1 and N_2 needed.



Schematic of vernier TDC



Switched Capacitor Array



"Time stretcher" GHz → MHz

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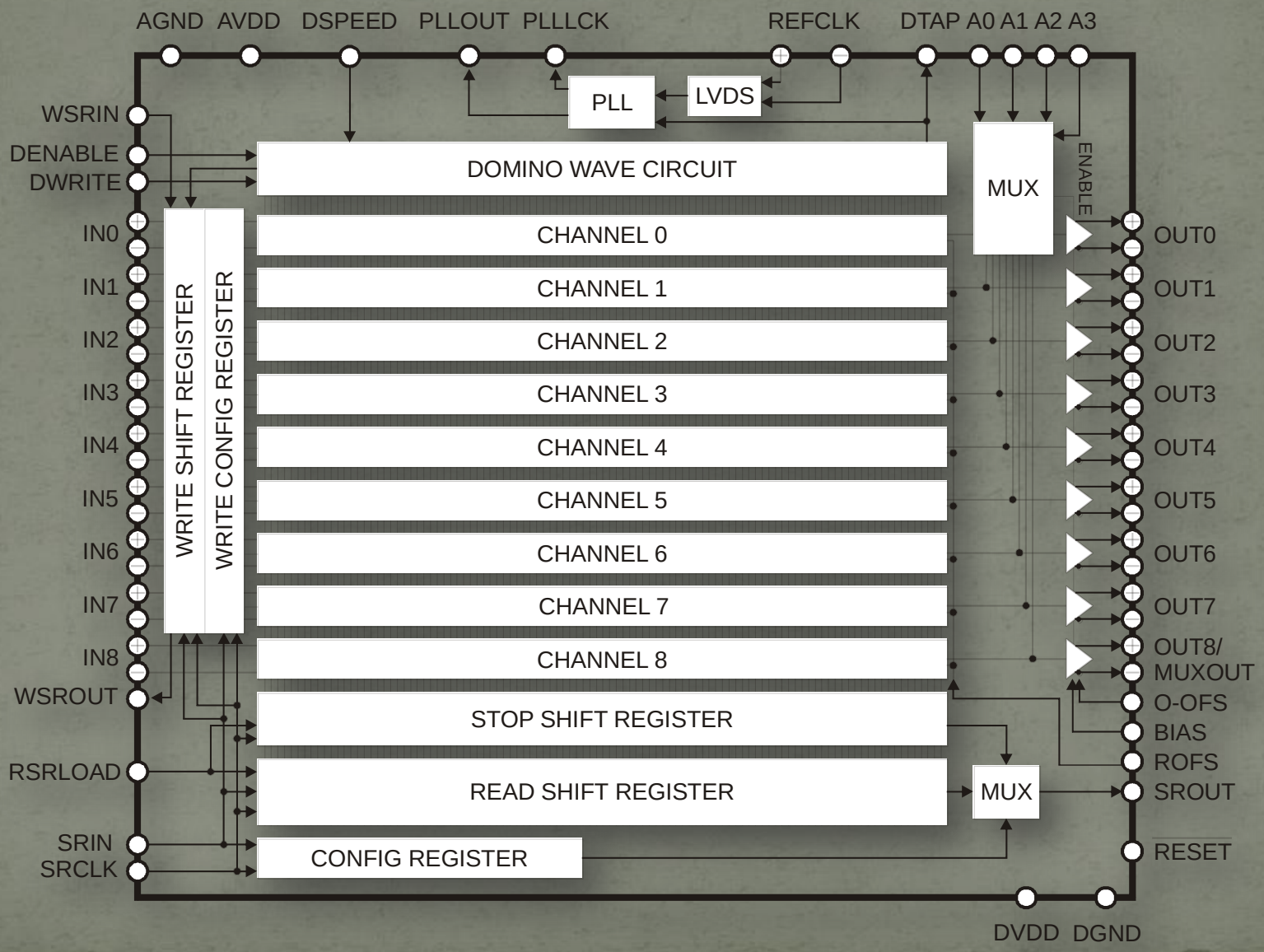
Functional block diagram of DRS4



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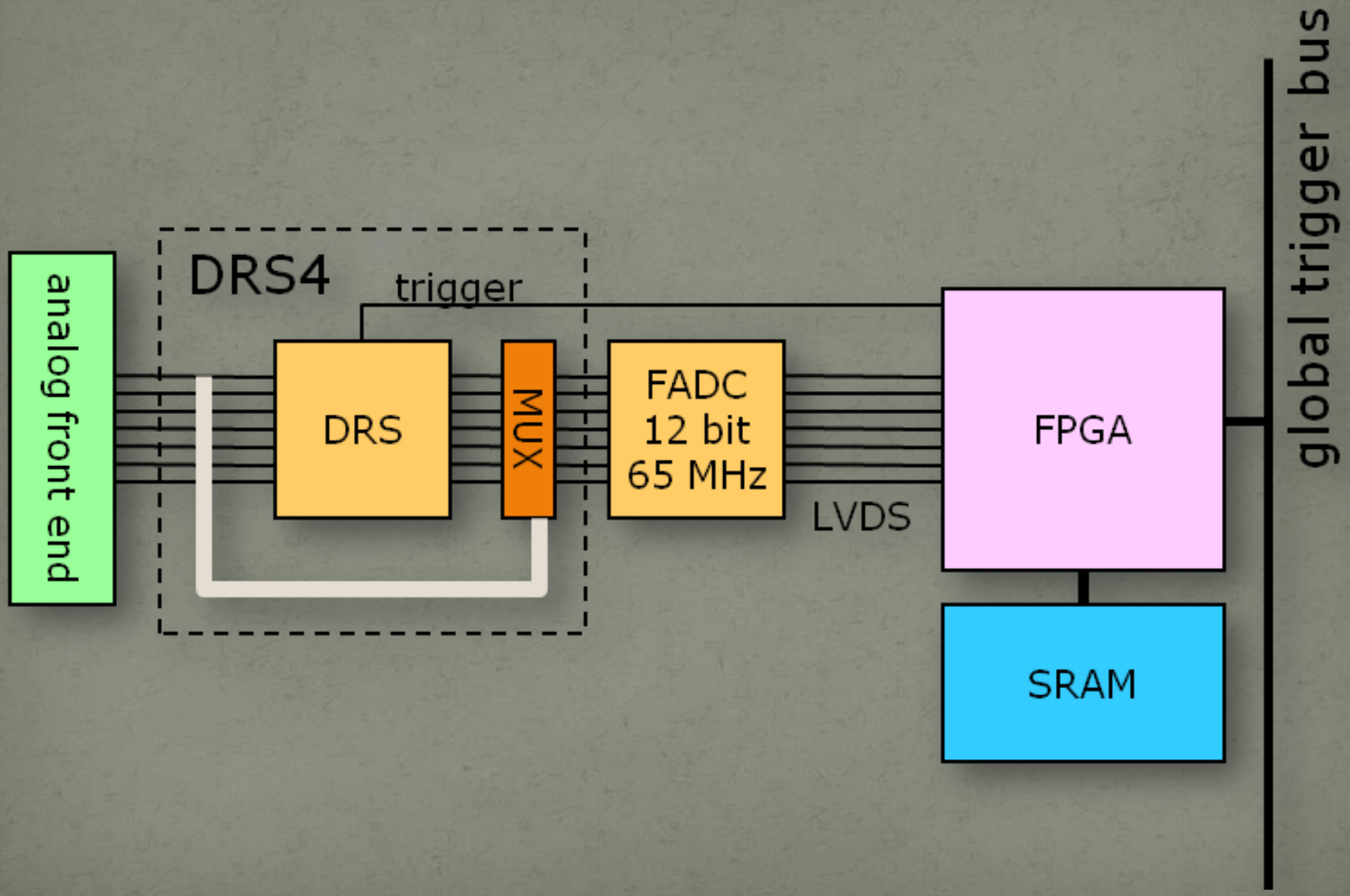
Data acquisition through DRS chip



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Thank you

For your attention.