DEVELOPMENT OF THE VME BASED DATA ACQUISITION SYSTEM

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Outline

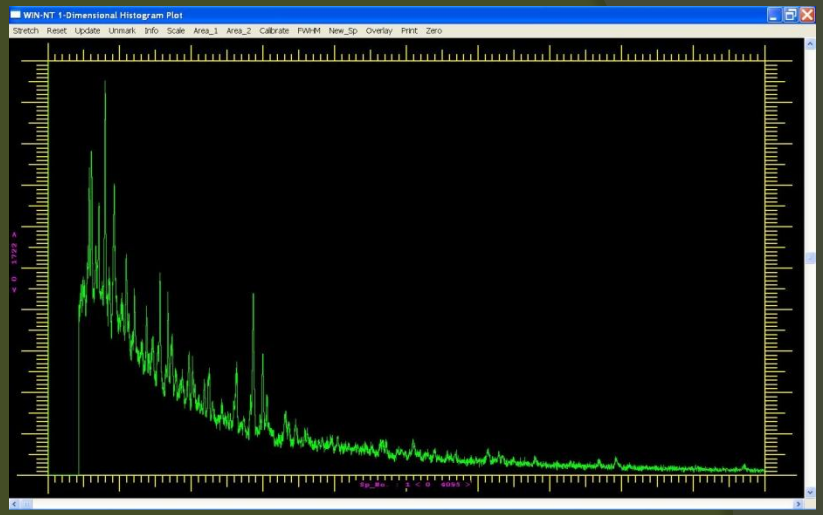
- DAQ Requirement
- DAQ Facilities
- VME DAQ
- Performance
- Synchronization
- Multicrate DAQ
- Future upgradation
- Conclusion

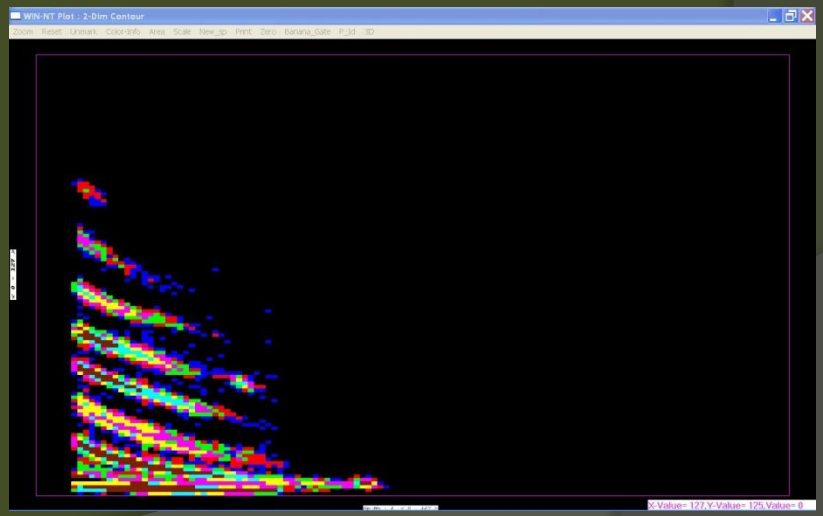
DAQ requirement for SCC experiments

- Large detector array with more than 1200 detector channels.
- More than 1Mparameter/sec of throughput required
- Multi-crate synchronization
- DAQ software should be capable of handling and monitoring multiple channels.

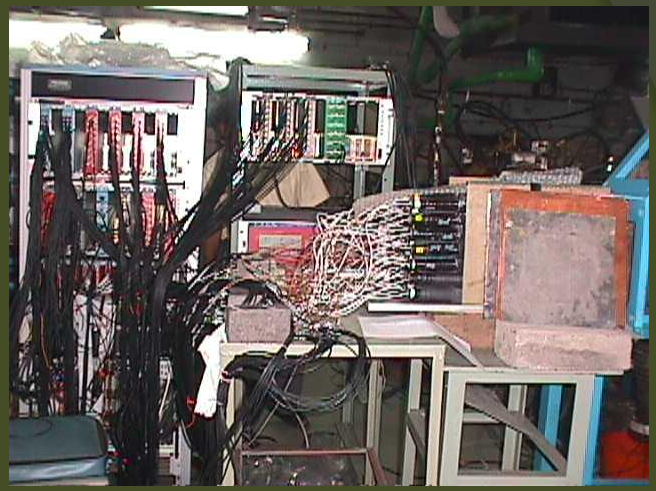
CAMAC DAQ Systems

- Win32 CAMAC DAQ with Hytec5331 CAMAC controller and Hytec1341 List Processor
- t4: First PC based Win16 Win3.1
- t32 for Win32 systems Windows 98/2000/NT/XP
- Offline version st32 and ast32

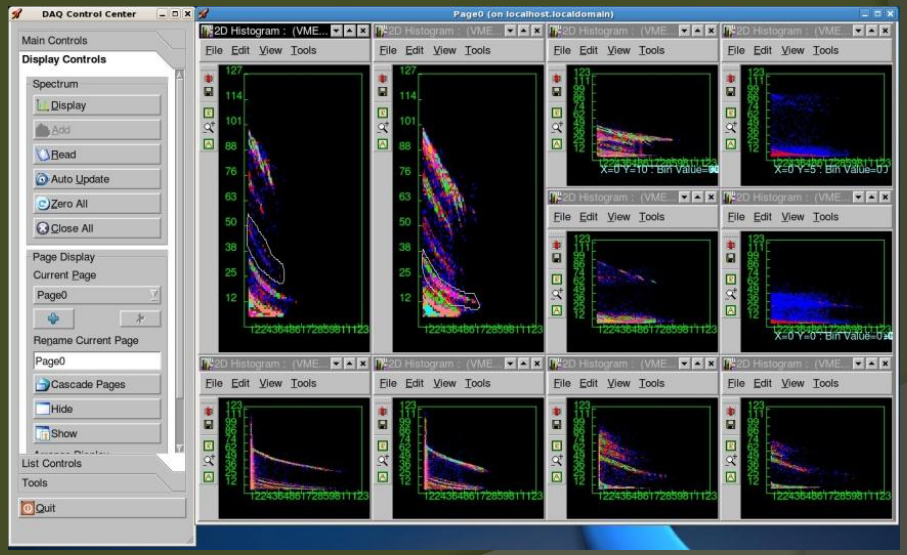




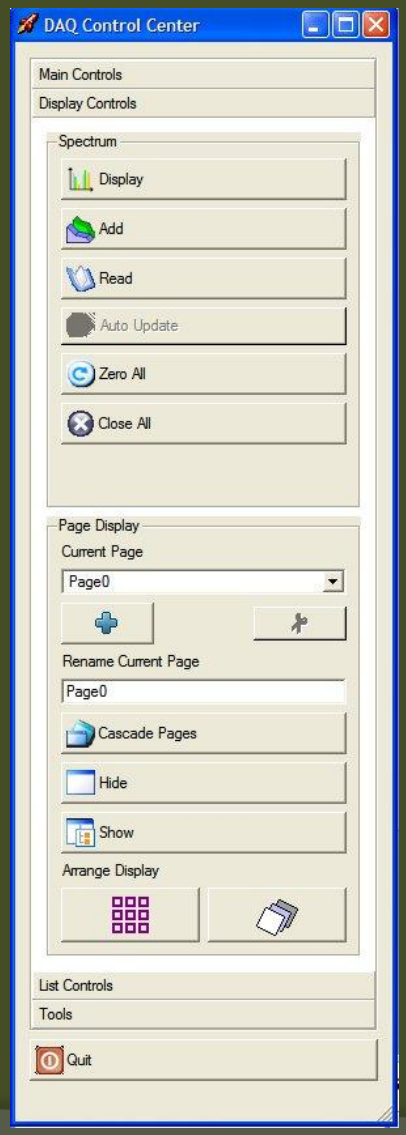
VME DAQ System

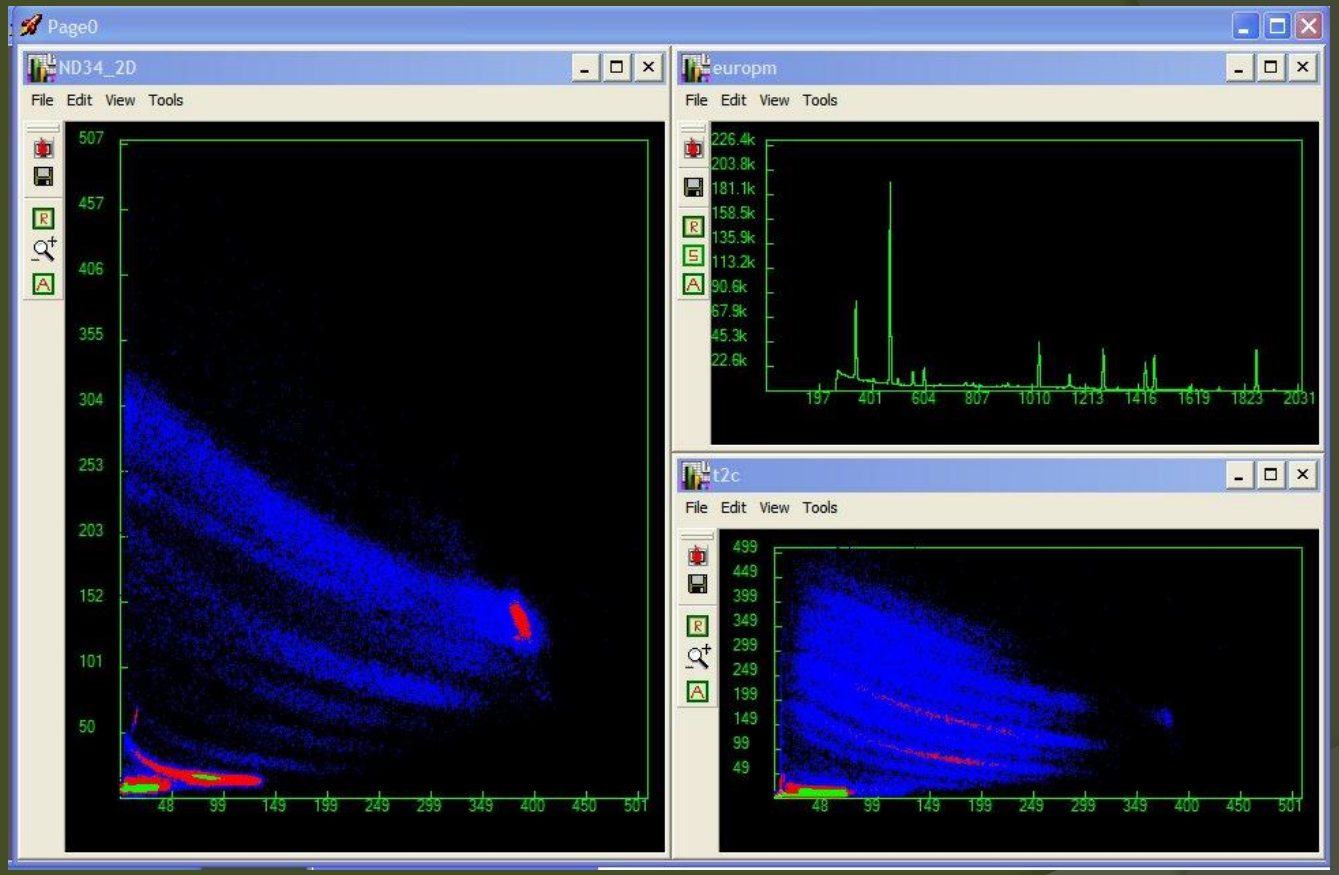


- The VME DAQ also supports CAMAC on both Linux and WindowsXP/2003
- CAMAC Peak sensing ADCs AD811, AD413, C420
- VME DAQ on Linux and WindowsXP/2003 with VME64 controller SIS3100, CAEN V2718
- VME785 ADC, VME775 TDC and VME792 QDC, Mesytec MDI2



VME DAQ Software





Configuration file

- C-style Single configuration file for complete configuration, compatible to both offline and online
- Define module, function, system, conditional construct

```
module{
                module_type=vme785;
                base_address=0x800000;
                instance=0;
               channel=32;
                conversion_gain=4096;
                event_size=34;
                geographical_address=4;
}
```

```
system{
 transfer_mode=CBLT;
 no_of_crates = 2;
event_trigger = 30;
}
```

```
function{
 func_type=oned;
 spec_len=4096;
 gain=1.0;
 offset=0.0;
 channel_no0{
    module_type=vme785;

    instance=0;
    channel=0;
   }
}
```

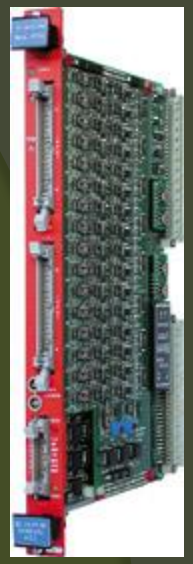
```
if(1 & 2)
{
 function{
    func_type=twod;
    x_len=512;
    y_len=512;
  channel_no0{
                module_type=vme785;
                instance=0;
                channel=16;
   }
  channel_no1{
                module_type=vme785;
                instance=0;
                channel=25;
   }
 }
}
```

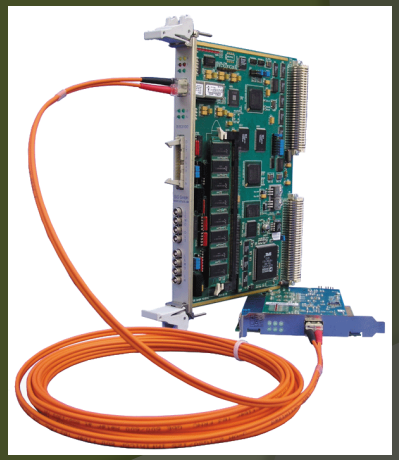
VME platform

- VME64 standard hardware
- VME is bus architecture, asynchronous mode of data transfer
- Address 32bit Data 32bit, 64bit address and data
- Basic VME cycle time 100ns
- In 32bit transfer mode maximum rate is 40MB/sec, in multiplex mode 80MB/sec
- Asynchronous transfer mode means the slowest module governs the speed.
- CAEN modules with 32 channel 32event FIFO maximum upto 7MB/sec has been achieved

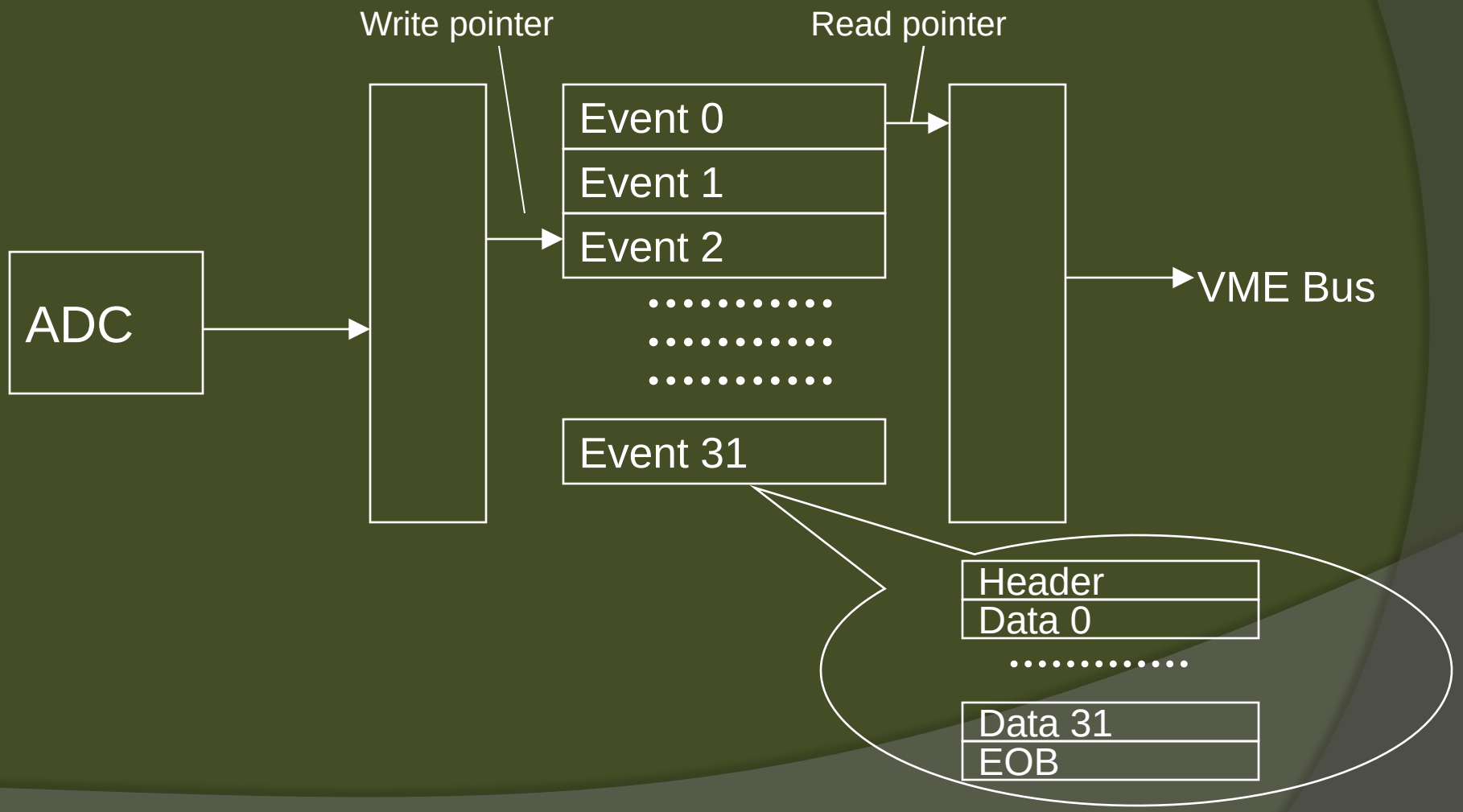
VME modules

- CAEN VME785, 792 & 775
  - 32 channel 12bit resolution
  - 5.7us ADC conversion time for all 32channels
  - 32event FIFO memory
  - External ECL bus for control and synchronization
  - BLT32, CBLT and MBLT capable
- MDI2 from mesytec





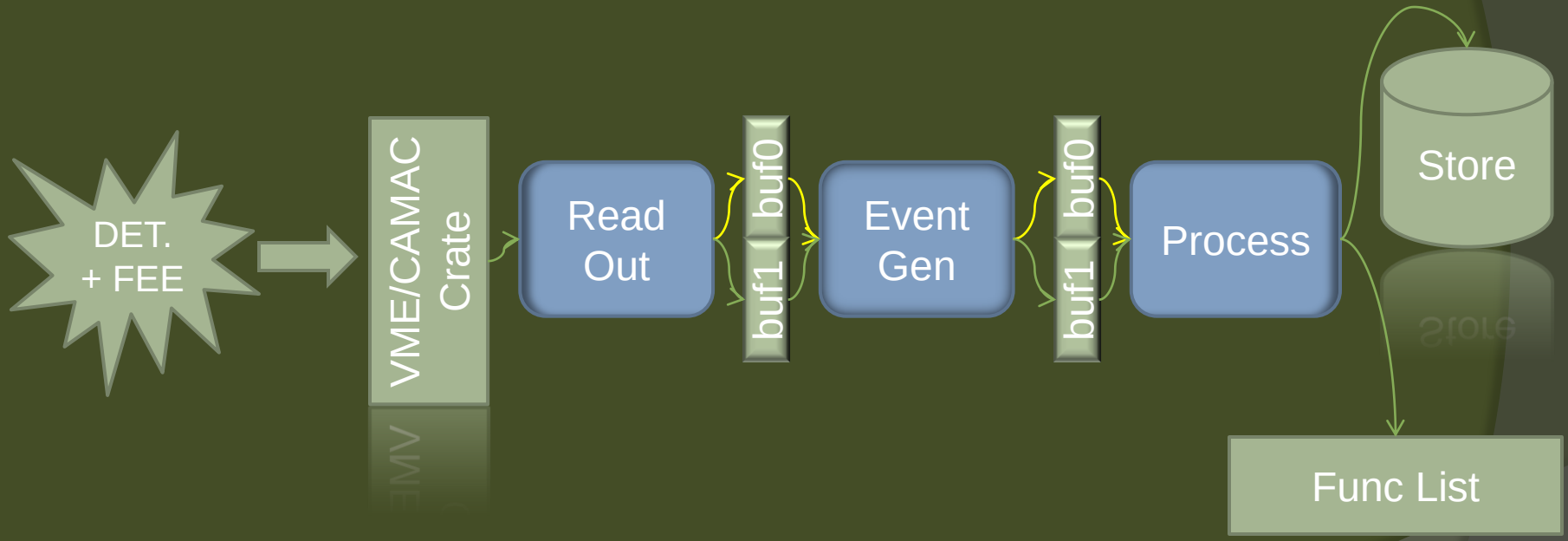
FIFO structure



Readout scheme

- Common busy mode
- Vertical Vs Horizontal readout
- Block transfer and chained block transfer (32 bits)
- Multiplexed block transfer and multiplexed chain block transfer(64 bits)

Multi-threaded Dataflow



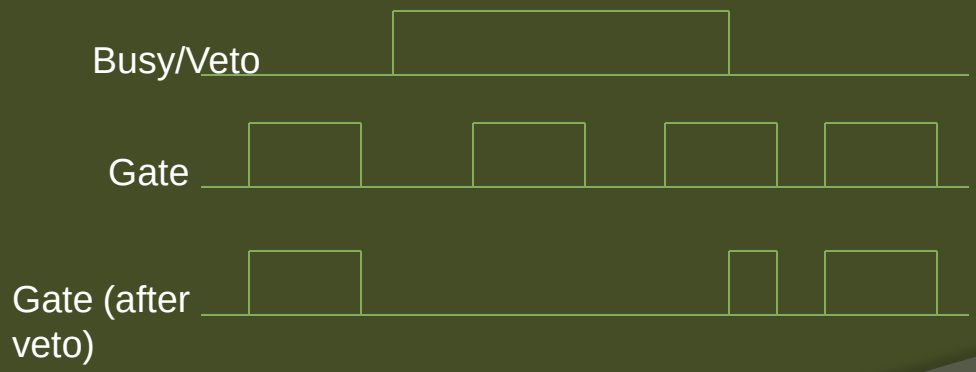
Dead time estimation

Gate Width (~3µs)	+	A/D conversion for N channels (5.7µs)	+	Tag and store data in FIFO (1µs)	+	Read data for N channels.	+	Process data for N channels.

- ✓ ~10µs is inherent for every valid gate
- ✓ 32 events can be stored into local FIFO, which can be read simultaneously
- ✓ Read time is divided into Fixed setup time + variable read time for N data
- ✓ Fixed dead time approximately 25µs for SIS & 60µs for CAEN with dual crate . It dominates when reading fewer channels
- ✓ Read & process can be operated in parallel threads.
- ✓ Maximum achieved rate with 3 modules was 840Kparameter/sec under application with SIS3100 controller

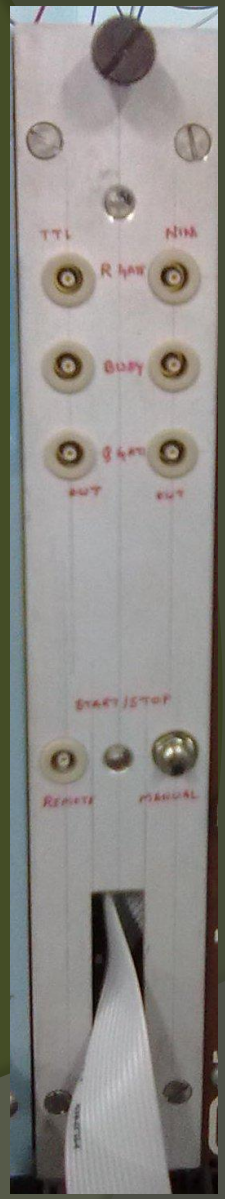
Synchronization

- Common busy method
  - All the module busy signals are wire-ORed
  - Any module busy will make the whole chain busy
  - Common busy can be used to veto the GATE signal



Custom built Synchronizer module

- NIM standard module
- NIM/TTL/ECL busy input
- NIM/TTL Gate input
- NIM/TTL/ECL Gate Output
- Module blocks all the gates in busy period and always preserves the gate width
- The module can be used for multi-crate synchronization



Multi-crate DAQ

- Multi-crate version of the DAQ is under development. Currently functional and performance testing is going on.
- 8 crates can be daisy chained with a single interface card
- Automatic CBLT setup for individual crates
- Synchronization is done by the custom built synchronizer module.
- Common dead time mode of operation

Future upgradation

- Parallel readout of crates may be implemented if proper driver support is available
- Multiple DAQ with independent readout is also possible by using suitable high resolution timestamp module
- A distributed DAQ with FPGA based digital filters is under development
- ASIC based FEE card with FPGA interface is also being explored for future upgradation

Conclusion

- CAMAC DAQ both on Linux (2.4 kernel) and WindowsXP/2003 is available
- VME DAQ single crate version is already in use, support available for selected modules and controllers
- Multicrate VME version will be released soon
- Prototype development for Digital filter based DAQ board is under development

Thank you